Fraunhofer
IISB

FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY IISB

Annual Report 2018

Fraunhofer Institute for Integrated Systems and Device Technology IISB

ANNUAL REPORT 2018

Imprint

Published by:
Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB
Schottkystrasse 10
91058 Erlangen, Germany

Editors:
Thomas Richter
Martin März

Layout and Setting:
Anja Grabinger
Helen Kühn
Thomas Richter

Printed by:
Frank UG Grafik – Druck – Werbung, Höchstadt

Printed on:
RecyStar® Nature, white, Recyclingpapier

Cover Photo:
Stationary electrical energy storage for peak shaving at Fraunhofer IISB.
© Kurt Fuchs / Fraunhofer IISB

ACHIEVEMENTS AND RESULTS

ANNUAL REPORT 2018

FRAUNHOFER INSTITUTE FOR

INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY IISB

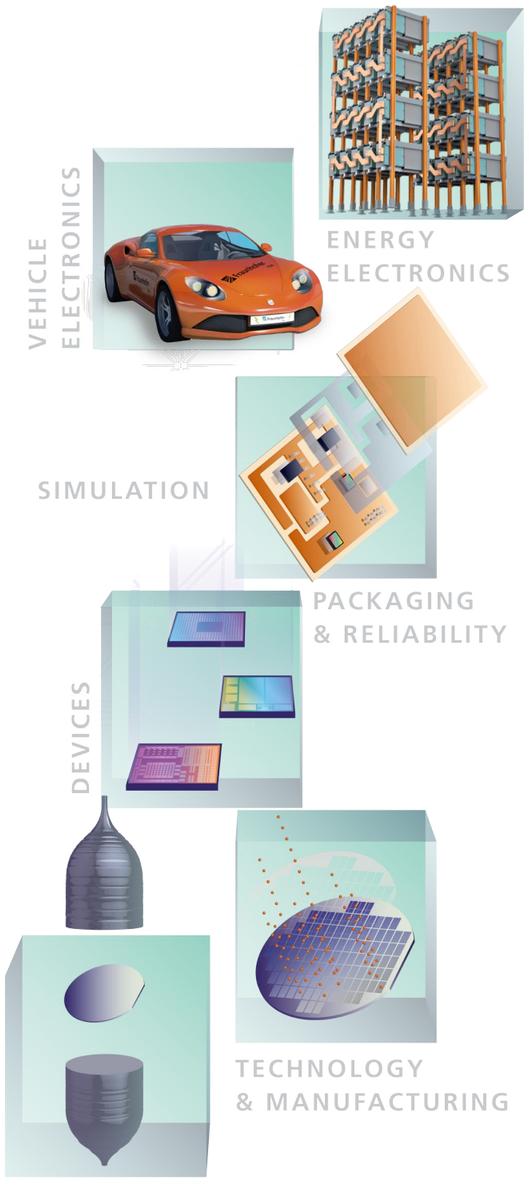
Director (acting):
Prof. Dr.-Ing. Martin März

Fraunhofer IISB
Schottkystrasse 10
91058 Erlangen, Germany

Phone: +49 (0) 9131 761-0
Fax: +49 (0) 9131 761-390

E-Mail: info@iisb.fraunhofer.de
Web: www.iisb.fraunhofer.de

PREFACE



1 *The R&D activities of Fraunhofer IISB cover the complete value chain for electronic systems, from basic materials to devices and modules up to application, with power electronics as a continuous backbone of the institute.*
© Fraunhofer IISB

2 *Prof. Dr.-Ing. Martin März, director of Fraunhofer IISB.*
© K. Fuchs / Fraunhofer IISB

Leading-Edge Power Electronic Systems and Technologies for Sustainable Mobility and Energy Supply. This is the core and credo of Fraunhofer IISB, which we will uphold and pursue in the sense of excellent research for our partners in industry and society.

For our institute, last year was marked by a profound and tragic event. Unbelievable for us all, our director, Prof. Dr. Lothar Frey, passed away in June 2018. We are very sad, and it is a particular incentive for us to continue the successful development of Fraunhofer IISB, which he deeply shaped, in his spirit.

Advanced materials engineering, comprehensive semiconductor device and processing technology, progressive packaging techniques, and elaborate system development for vehicles and energy grids span the broad spectrum of R&D at Fraunhofer IISB. Our work is explicitly dedicated to meet the global challenges of digitalization, energy efficiency, and climate protection, and to further intensify the transfer of scientific results to industrial implementation. The latter is especially addressed by our collaboration within the Leistungszentrum Elektroniksysteme (LZE). Our membership in the Forschungsfabrik Mikroelektronik Deutschland (FMD) allows us to contribute our special expertise in silicon carbide (SiC) and other wide-bandgap semiconductors, as well as in power module packaging, testing, and reliability to a powerful research network.

Our proven approach of Cognitive Power Electronics 4.0 takes power electronic systems into the age of digitalization and significantly expands their functionalities in intelligent control, prediction, and maintenance on a superior scale. Our last IISB Annual Conference in autumn focused on decentralized energy systems for industrial environments, dealing with the efficient linkage of electrical and various non-electrical generators, storages, and consumers of energy. The launch of our medium-voltage application hall and other laboratories in our new extension building in Erlangen will further enhance our capabilities in this area. The organization of the 22nd International Conference on Ion Implantation Technology (IIT 2018) in Würzburg underscores our deep embedding in the electronics research community.

I would like to thank all my colleagues for their excellent work and the trusting cooperation in the past year. I also thank our partners in industry and all our funding authorities, especially the Bavarian Ministry of Economic Affairs, Regional Development and Energy as well as the German Federal Ministry of Education and Research (BMBF), for their support. I now cordially invite you to take a look at the work of Fraunhofer IISB presented in this report.

Sincerely yours,
Prof. Dr. Martin März (Erlangen, April 2019)

TABLE OF CONTENTS

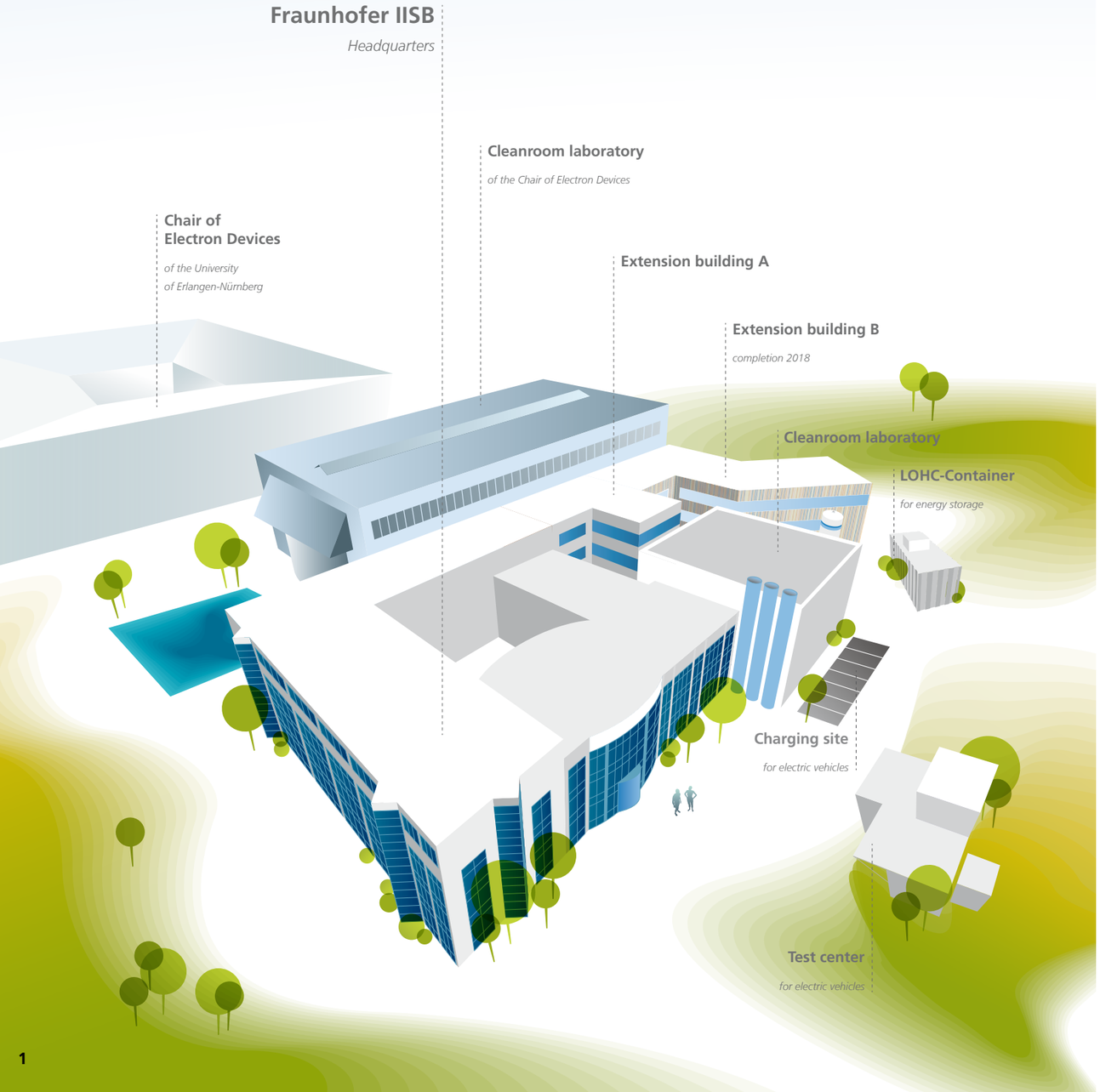
The „Names and Data" chapter is exclusively available in the online version of the annual report:

https://www.iisb.fraunhofer.de/annual_reports

It includes the following contents:

- Guest Scientists
- Patents
- Conferences, Workshops, Fairs, and Exhibitions
- Publications
- Presentations
- PhD Theses
- Master Theses
- Bachelor Theses

FRAUNHOFER IISB AT A GLANCE



1

PROFILE AND HISTORY

PROFILE

The Fraunhofer Institute for Integrated Systems and Device Technology IISB conducts applied research and development in the field of electronic systems for application in, e.g., electric vehicles or energy technology. In this connection, the IISB extensively covers the complete value chain from basic materials to entire power electronic systems. With its two business areas, semiconductors and power electronics, the institute provides innovation and solutions in materials development, semiconductor technology and manufacturing, devices and modules, as well as in system development for vehicle power electronics, energy electronics, and energy infrastructures. This is supplemented by broad activities in reliability, simulation, characterization, and metrology.

The headquarters of the IISB is located in Erlangen, Germany. The institute has branches in Nuremberg, Freiberg, and Chemnitz. As one of the 72 institutes of the Fraunhofer-Gesellschaft, the IISB does contract research for industry and public authorities. Moreover, it closely cooperates with the University of Erlangen-Nürnberg. The IISB has more than 250 employees plus numerous students working as research assistants. The institute is equipped with high-class laboratories, such as a test center for electric cars and an application center for DC grid technology. Together with the University, it operates 1500 m^2 of cleanroom area for semiconductor technology on silicon and silicon carbide.

The IISB is a close partner of national and international industry. Its main objective is to provide excellent research to its customers and to set technological benchmarks as one of the leading research institutions in electronic systems. Cooperation includes research and development projects, prototyping, consultancy, licensing, and studies.

HISTORY

The Fraunhofer Institute for Integrated Systems and Device Technology IISB in Erlangen is an important center of applied R&D for electronic systems, power electronics, semiconductor technology, and materials development in the Nuremberg metropolitan region, Germany, and Europe. It was founded in 1985 as the Electron Devices department AIS-B of the Fraunhofer Working Group for Integrated Circuits. In 1993, it became a Fraunhofer institute (IIS-B), but was still formally linked to its sibling institute IIS-A, today's Fraunhofer Institute for Integrated Circuits IIS. In 2003, IIS and IISB became completely independent from each other as two individual Fraunhofer institutes. From 1985 until his retirement in 2008, Prof. Heiner Ryssel was the head of the IISB. Since 2008 Prof. Lothar Frey has been director of the institute. From the beginning, the institute has been closely cooperating with the University of Erlangen-Nürnberg (FAU). In 2015, IISB together with IIS and FAU founded the "Leistungszentrum Elektroniksysteme" (LZE).

1 *Schematic overview of Fraunhofer IISB headquarters in Erlangen.*
© Fraunhofer IISB

ORGANIZATIONAL CHART 2018

DIRECTOR
M. März (acting)

H. Hermes — ADMINISTRATION	J. Schöneboom — INFRASTRUCTURE
B. Fischer — STRATEGY & PR	G. Ardelean — IT

SIMULATION J. Lorenz	MATERIALS J. Friedrich	TECHNOLOGY & MANUFACTURING A. Bauer	DEVICES & RELIABILITY A. Schletz	VEHICLE ELECTRONICS B. Eckardt	INTELLIGENT ENERGY SYSTEMS V. Lorentz
DOPING & DEVICES P. Pichler	SILICON C. Reimann	π-FAB V. Häublein	DEVICES T. Erlbacher	DRIVES & MECHATRONICS M. Hofmann	INDUSTRIAL POWER ELECTRONICS M. Billmann
STRUCTURE SIMULATION E. Bär	SILICON CARBIDE P. Berwian	THIN-FILM SYSTEMS M. Jank	PACKAGING C.Bayer	AC/DC CONVERTERS S. Zeltner	BATTERY SYSTEMS V. Lorentz
LITHOGRAPHY & OPTICS A. Erdmann	NITRIDES E. Meißner	NANO TECHNIQUES M. Rommel	TEST & RELIABILITY A. Schletz	DC/DC CONVERTERS S. Matlok	DC GRIDS B. Wunder
AI-AUGMENTED SIMULATION A. Roßkopf	ENERGY MATERIALS U. Wunderwald	MANUFACTURING CONTROL M. Pfeffer		RF POWER & EMC B. Eckardt	ENERGY TECHNOLOGIES R. Öchsner
	MATERIAL QUALIFICATION F. Beyer			GRID INTERFACES S. Endres	DATA ANALYTICS M. Schellenberger
	EQUIPMENT SIMULATION J. Friedrich			AIRCRAFT ELECTRONICS F. Hilpert	
				MEDIUM VOLTAGE ELECTRONICS T. Heckel	

ADVISORY BOARD 2018

IISB is consulted by an Advisory Board, whose members come from industry and research:

Dr. Stefan Kampmann (Chairman of the Advisory Board)
OSRAM Licht AG

Dr. Helmut Gassel
Infineon Technologies AG

Thomas Harder
European Center for Power Electronics (ECPE)

Prof. Dr. Reinhard Lerch
Friedrich-Alexander-Universität Erlangen-Nürnberg

Markus Lötzsch
Nuremberg Chamber of Commerce and Industry

MinR Dr. Stefan Mengel
Federal Ministry of Education and Research (BMBF)

Petra Mönius
Conti Temic microelectronic GmbH

Dr. Andreas Mühe
PVA Crystal Growing Systems GmbH

Dr. Martin Schrems
AT&S AG

Dr. Karl-Heinz Stegemann
X-FAB Dresden GmbH & Co. KG

Dr. Thomas Stockmeier
ams AG

MR Dr. Stefan Wimbauer
Bavarian Ministry of Economic Affairs, Regional Development and Energy

RESEARCH AREAS

The R&D activities of the IISB cover the complete value chain for electronic systems, from basic materials to devices and modules up to application, with power electronics as a continuous backbone of the institute.

MATERIALS

Together with its industrial partners, Fraunhofer IISB develops equipment and processes for the production of crystalline bulk and layer materials for electronics. This comprises silicon, wide-band-gap semiconductors (e.g., silicon carbide, gallium nitride), materials for optical applications, detectors, and energy technology.

TECHNOLOGY & MANUFACTURING

The IISB operates extensive semiconductor technology lines, cleanroom infrastructure, and metrology on silicon and silicon carbide for the development of custom-tailored processes and prototype devices in power electronics and microelectronics. Furthermore, IISB works on nanotechniques, particle and thin-film systems. Manufacturing aspects such as process and quality control, equipment optimization, automation, and efficiency are also considered.

SIMULATION

The research activities of the IISB and its customers are supported by extensive competencies in simulation, modeling, and software development in the fields of, e.g., process and device simulation in semiconductor technology, crystal growth simulation, or thermal simulation for designing power electronic systems.

DEVICES

The institute develops customer-specific active and passive electron devices on silicon and silicon carbide for application in power electronics, microelectronics, and sensors. This includes novel device concepts and the development of cost-efficient processes tailored towards implementation and realization of customized products.

PACKAGING & RELIABILITY

New methods and materials for packaging, cooling, lifetime and failure analysis, and reliability play an important role. At IISB, packaging and reliability research are closely combined with each other. By analyzing the exact failure mechanisms after lifetime and reliability tests, the joining technologies, materials, concepts and mechanical designs are further improved. On the other hand, new packaging designs have a direct impact on the test methodologies and accelerating factors.

VEHICLE ELECTRONICS

Efficient, compact, and robust power electronic systems for all kind of vehicles are in the focus of the IISB. This comprises electric drives, battery systems, and the charging infrastructure of electric cars. Benchmark values for energy efficiency and power density are regularly set for the work of the IISB. Further fields of application are shipping and aviation.

ENERGY ELECTRONICS

Power electronic systems are indispensable for realizing a modern energy supply and the transition to predominantly regenerative energy sources. The developments of the IISB contribute to this on all levels of the power grid through, e.g., electronic components for HV DC transport, local DC micro grids or the integration of electrical storages and regenerative sources in the power grid.

ENERGY INFRASTRUCTURE TECHNOLOGIES

The goal of this field of activity is the coupling of electric and non-electric energy and the development of the necessary interfaces for implementing a sustainable energy infrastructure, especially for industry-size environments.

LOCATIONS

HEADQUARTERS OF FRAUNHOFER IISB ERLANGEN

Schottkystrasse 10, 91058 Erlangen

The headquarters of Fraunhofer IISB in Erlangen are located close to the University of Erlangen-Nürnberg. About 7000 m² of laboratories and office area allow research and development on a broad range of power electronics, semiconductor technology, and materials development. A test center for electric cars and extensive cleanroom area for semiconductor technology on silicon and silicon carbide, which is partly operated together with the Chair of Electron Devices of the University, are part of the available infrastructure.

BRANCH LABS OF FRAUNHOFER IISB

Fraunhofer IISB Nuremberg-EnCN
Fürther Strasse 250, "Auf AEG", 90429 Nuremberg

As a member of the "Energie Campus Nürnberg" (EnCN), the IISB operates a 450 m² branch lab on megawatt power electronics for energy supply in the joint EnCN building in Nuremberg.

Technology Center for Semiconductor Materials THM Freiberg
Am St.-Niclas-Schacht 13, 09599 Freiberg

The THM is a joint department of Fraunhofer IISB and Fraunhofer ISE. It supports industry in technologies for the production of innovative semiconductor materials to be used in microelectronics, optoelectronics, and photovoltaics. The IISB part of the THM comprises 650 m².

NETWORK AND PARTNERS

Within its research activities, Fraunhofer IISB pursues cooperation with numerous national and international partners in joint projects and associations, among others:

- Since its foundation, the IISB has been closely cooperating with the University of Erlangen-Nürnberg. The institute is directed by the head of the Chair of Electron Devices of the University. The joint operation of infrastructure as well as the exchange in education and training create extensive synergies.
- The IISB is a core member of the "Leistungszentrum Elektroniksysteme" (www.leistungszentrum-elektroniksysteme.de, www.lze.bayern).
- The IISB is the coordinator of the Bavarian energy research project SEEDs (www.energy-seeds.org).
- The IISB is a member of the "Energie Campus Nürnberg" (EnCN, www.encn.de).
- The IISB is the coordinator of the Fraunhofer Innovation Cluster "Electronics for Sustainable Energy Use".
- The IISB is a partner of the excellence projects at the University of Erlangen-Nürnberg (www.eam.uni-erlangen.de, www.aot.uni-erlangen.de/saot/).
- The IISB closely cooperates with industry and research associations, such as the European Center for Power Electronics, the Bavarian Clusters for Power Electronics and Mechatronics & Automation, or the German Crystal Association DGKK e.V.
- The IISB is the coordinator and partner, respectively, of numerous European research projects.
- Together with the Federal Ministry for Education and Research (BMBF), the IISB initiated and operates the joint student program of BMBF and Fraunhofer for electric mobility, DRIVE-E (www.drive-e.org).
- The IISB is a close partner of the "Förderkreis für die Mikroelektronik e.V."

The IISB is member of the following Fraunhofer groups and alliances:

- Fraunhofer Group for Microelectronics (www.mikroelektronik.fraunhofer.de)
- Fraunhofer Energy Alliance (www.energie.fraunhofer.de)
- Fraunhofer Battery Alliance (www.batterien.fraunhofer.de)
- Fraunhofer Nanotechnology Alliance (www.nano.fraunhofer.de)

NETWORK AND PARTNERS

1 *Chair of Electron Devices of the University of Erlangen-Nürnberg: main building and clean room laboratory.*
© LEB

CHAIR OF POWER ELECTRONICS (LEE), UNIVERSITY OF ERLANGEN-NÜRNBERG

Since September 1, 2016, Prof. Dr. Martin März, deputy director at Fraunhofer IISB, is heading the Chair of Power Electronics (LEE). The chair conducts research on current topics in the field of power electronics for the electric power supply. Beside stationary decentralized electrical power systems, the addressed application fields also include the power-nets in vehicles, ships, railways, and airplanes. LEE is part of Energy Campus Nuremberg (EnCN) on the former AEG company grounds in the Fürther Strasse in Nuremberg, and the first chair grown out of the EnCN.

CHAIR OF ELECTRON DEVICES (LEB), UNIVERSITY OF ERLANGEN-NÜRNBERG

The Fraunhofer IISB and the Chair of Electron Devices (German abbreviation: LEB) of the University of Erlangen-Nürnberg are both headed by Prof. Lothar Frey.

Within the framework of a cooperation agreement, the two institutions not only jointly operate the University's cleanroom hall and other laboratories but also work closely together with regard to teaching and research.

The cooperation of the Chair of Electron Devices and the Fraunhofer IISB makes it possible to cover the entire chain of topics from basic research to the transfer to industry. For many years, the vocational training as a "microtechnologist" has been offered jointly by IISB and the Chair of Electron Devices. Employees of IISB assist in courses and internships at the University.

The following staff members of Fraunhofer IISB regularly give lectures at the University of Erlangen-Nürnberg:

Dr. Andreas Erdmann
- Optical Lithography: Technology, Physical Effects, and Modeling

Dr. Tobias Erlbacher
- Semiconductor Power Devices

Prof. Dr. Lothar Frey
- Nanoelectronics
- Process Integration and Components Architecture
- Semiconductor Devices
- Technology of Integrated Circuits

Dr. Michael Jank
- Introduction to Printable Electronics
- Nanoelectronics

Dr. Jürgen Lorenz
- Process and Device Simulation

Prof. Dr. Martin März
- Power Electronics for Decentralized Energy Supply - DC Grids
- Power Electronics in Vehicles and Electric Powertrains
- Thermal Management for Power Electronics

Prof. Dr. Lothar Pfitzner
- Semiconductor Equipment Technics

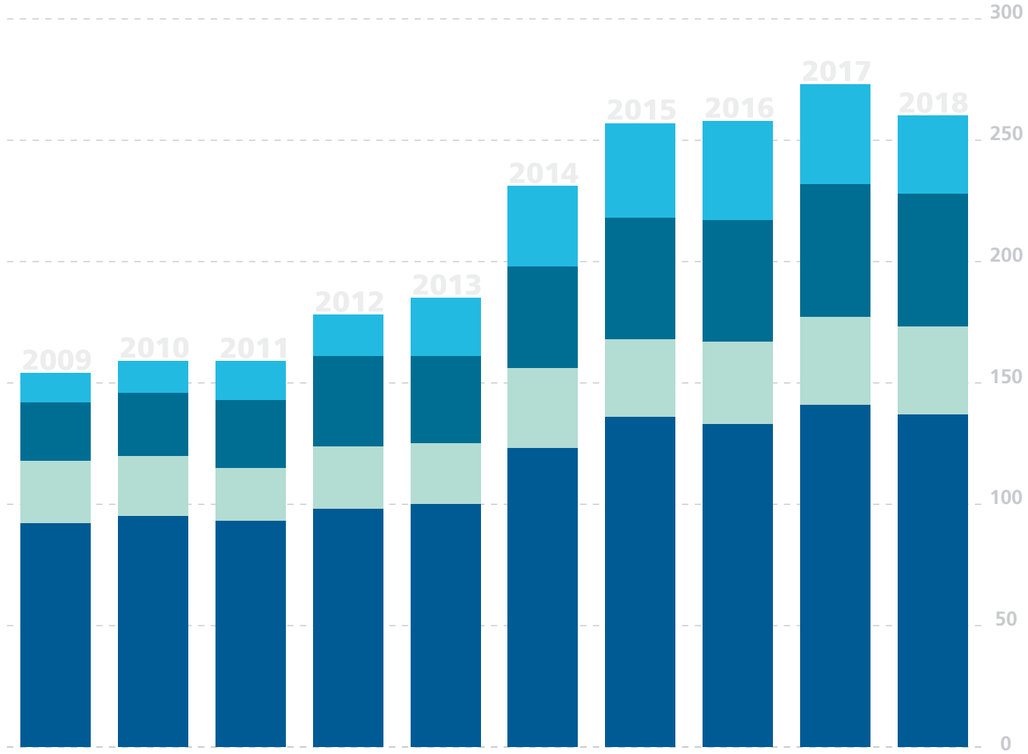
Priv.-Doz. Dr. Peter Pichler
- Reliability and Failure Analysis of Integrated Circuits

NUMBERS AND STATISTICS

STAFF DEVELOPMENT

260 Employees in 2018

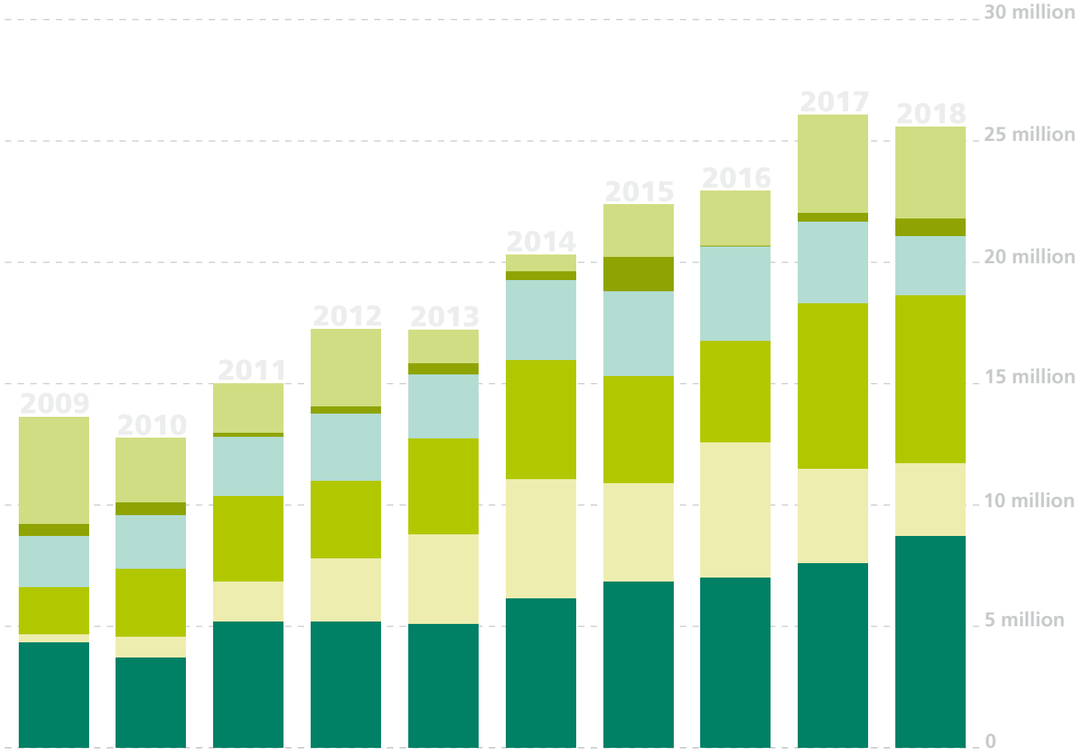
- Scientists
- Technicians
- Office Staff and Others
- Student Assistants equiv.



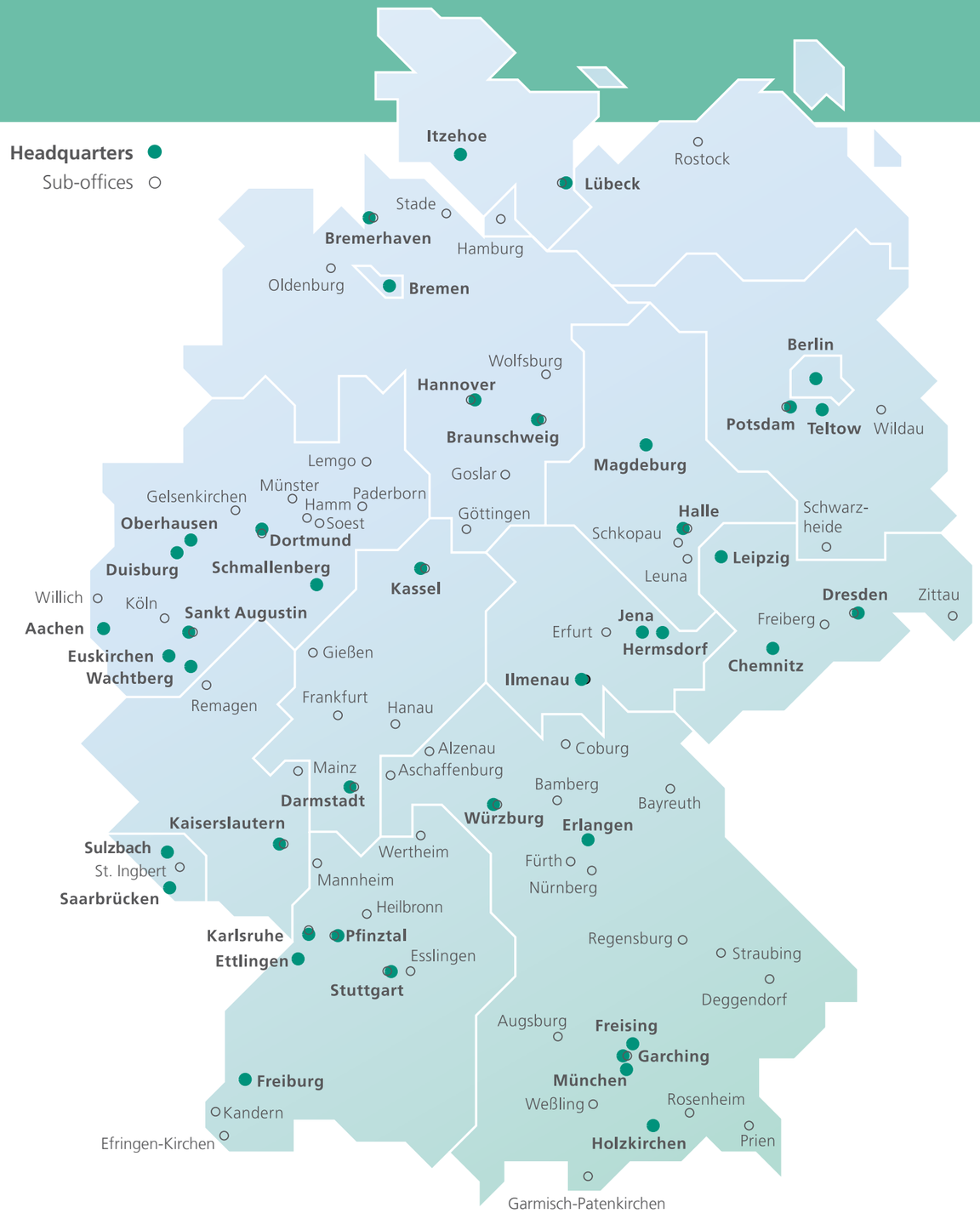
OPERATING BUDGET

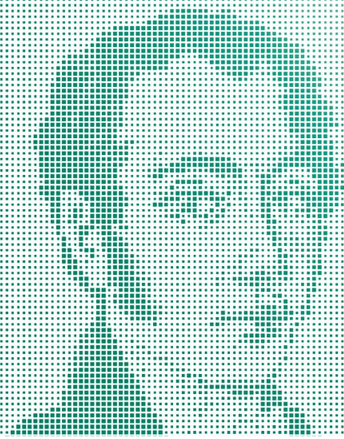
25 589 000 Euro in 2018

- Basic Funding
- Int. Programs
- EU + Others
- Federal
- Bavaria + Saxony
- Industrial Partners



FRAUNHOFER





THE FRAUNHOFER-GESELLSCHAFT

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector, and public administration.

At present, the Fraunhofer-Gesellschaft maintains 72 institutes and research units. The majority of the more than 25,000 staff are qualified scientists and engineers, who work with an annual research budget of 2.3 billion euros. Of this sum, almost 2 billion euros is generated through contract research. Around 70 percent of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Around 30 percent is contributed by the German federal and state governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

International collaborations with excellent research partners and innovative companies around the world ensure direct access to regions of the greatest importance to present and future scientific progress and economic development.

With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor, and entrepreneur.

1 *Locations of the Fraunhofer-Gesellschaft in Germany.*
© Fraunhofer

2 *Joseph von Fraunhofer (1787 – 1826): researcher, inventor, entrepreneur.*
© Fraunhofer IISB

RESEARCH FAB MICROELECTRONICS GERMANY

1

ONE-STOP-SHOP FOR THE COMPLETE MICRO AND NANOELECTRONICS VALUE CHAIN

The Fraunhofer IISB is one of 13 members of the Research Fab Microelectronics Germany (FMD) – Europe's largest cross-location R&D collaboration for microelectronics and nanoelectronics, with over 2000 scientists.

Within this new type of cooperation, the advantages of two strong and decentralized research organizations – the Fraunhofer-Gesellschaft and the Leibniz Association – are combined with the synergies of a central organization to form the world's most capable provider of applied research, development, and innovation within microelectronics and nanoelectronics. The close intermeshing and the uniform public face allow the FMD to serve not only customers from heavy industry, but also to offer SMEs and startups more comprehensive and simpler access to the next generation of technology.

The German Federal Ministry of Education and Research (BMBF) is funding the setup of the FMD to the tune of 350 million euros, largely in the modernization of the institutes' research equipment. With this funding, the BMBF intends to strengthen the innovativeness of the German and European semiconductor and electronics industry and is supporting the initiative with the largest investment in research devices since Germany was reunified.

A year and a half after the project started on April 6th, 2017, a lot of new acquisitions for the modernization of the laboratory facilities at FMD's locations around Germany went into operation. The ceremonial opening of the first integration line was on September 28th, 2018, as part of the 1st FMD Innovation Day at the Berlin-based Fraunhofer Institute for Reliability and Microintegration IZM, which hosted the event on behalf of all members.

At around the halfway point of the project, 45 percent of the planned investments for the FMD have been successfully fulfilled.

The setup of the Research Fab Microelectronics Germany is coordinated in a central business office in Berlin, although – true to the concept of a virtual organization – additional locations in Dresden and Munich have also been opened. The FMD business office is the central contact point for potential and existing customers and is thus a significant driver of the development of the business in the area of microelectronics and nanoelectronics.

In order to be able to offer nationally coordinated technology and system developments from a single provider, the technological expertise of the institutes was grouped into six overarching areas – the technology platforms known as Microwave and Terahertz / Power Electronics / Extended CMOS / Optoelectronic Systems / Sensor Systems / MEMS Actuators. Within these technology platforms, the FMD offers the market technological developments along the entire value creation chain, from system design to testing and reliability.

In addition to these technologically oriented offerings, the FMD also offers cross-institute application solutions from a single provider. This offers customers a way of realizing combined and optimized system solutions together the FMD and its institutes. In doing so, the Research Fab works in synergy with the business units of all institutes involved. We, as the FMD, can thus offer our customers a wider range of application solutions.

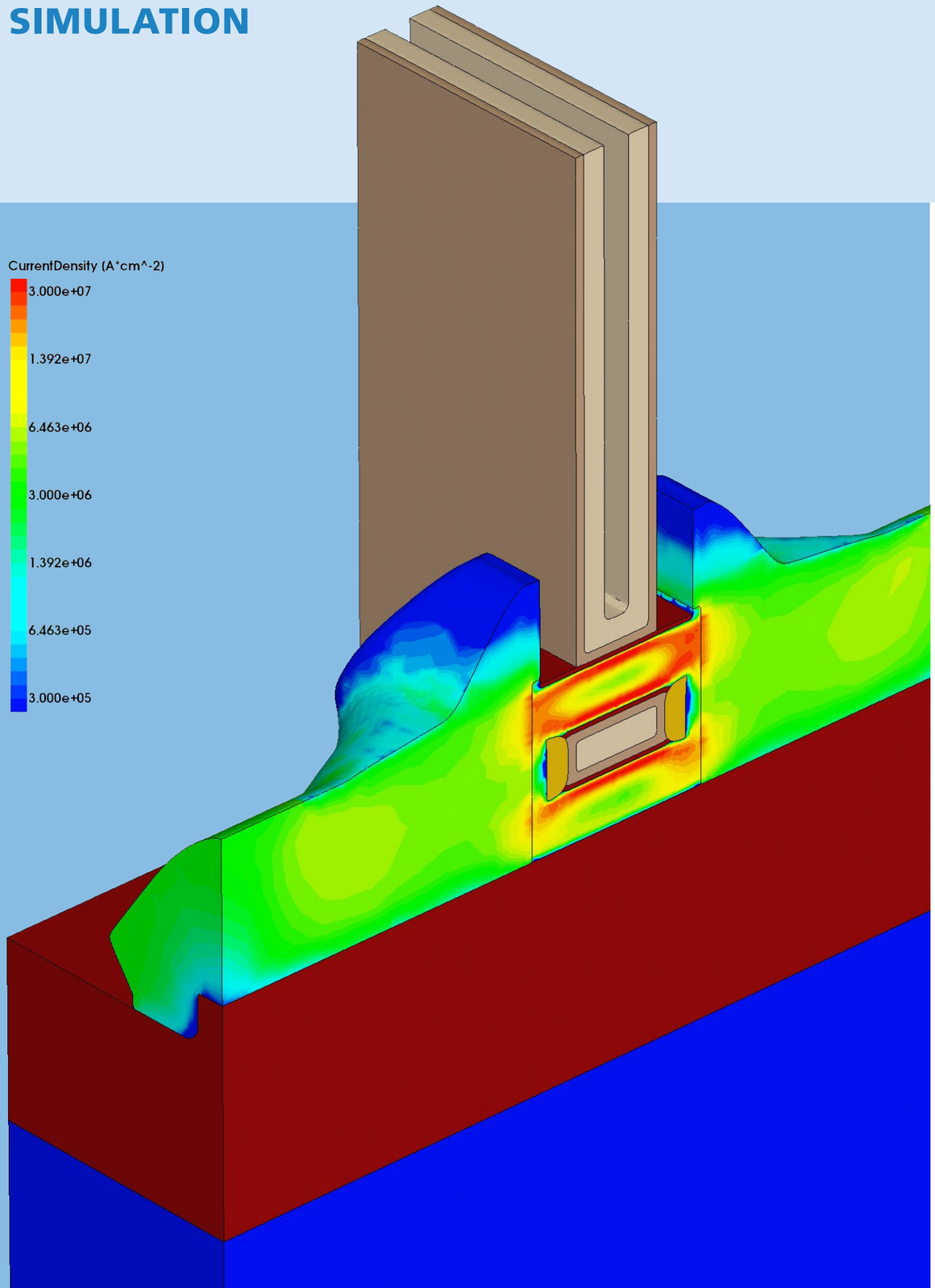
In 2017, successful project involvements were set up and orders were completed in combination with the FMD. For 2018, projects based on the FMD investments with a volume of 41.1 million euros can already be identified, which represents a significant success at such an early stage. The industrial share of this project volume is already at 30 percent, which highlights the importance of this unique cooperation in German microelectronics research to industry.

In 2019, the Research Fab Microelectronics Germany will enter the next phase. After establishment and structuring of the organization, the largest cross-location R&D collaboration for microelectronics and nanoelectronics in Europe, in partnership with its institutes, will prove its mettle on the market.

You will find more information about the Research Fab Microelectronics Germany here:

1 *Full steam ahead – at the opening ceremony of the first FMD integration line. From left to right: Prof. Matthias Kleiner, President of the Leibniz Association; Prof. Georg Rosenfeld, former member of the board of the Fraunhofer-Gesellschaft; Prof. Hubert Lakner, Chairman of the Steering Committee of the Research Fab Microelectronics Germany; and Dr. Michael Meister, parliamentary undersecretary at the Federal Ministry of Education and Research (BMBF).*
© U. Steinert / Fraunhofer

SIMULATION



1

2

1 *Simulated current density in a field effect transistor structure with two nanowires.*

2 *Dr. Jürgen Lorenz, head of the Simulation department. © K. Fuchs / Fraunhofer IISB*

Modeling and simulation has during the last decades established itself as indispensable for the development and optimization of technologies and applications in most industrial areas. Its methods range from first-principle calculations frequently done on the atomic or molecular scale to large-area simulations using heuristic models which do not solve detailed physical equations but employ simplified analytical expressions and elaborated methods for extraction of the parameters required. In micro and nanoelectronics, the simulation of semiconductor fabrication processes, devices, circuits, and systems greatly contributes to the reduction of development costs in the semiconductor industry. Among others, this has been confirmed for micro- and nanoelectronics in the International Technology Roadmap for Semiconductors (ITRS). The department "Modeling and Artificial Intelligence" contributes to this by developing physical models and programs for the simulation and optimization of semiconductor fabrication processes and equipment. Furthermore, it supports the development of lithography (incl. masks, materials, and imaging systems) and other processes, devices, circuits, and systems by providing and applying its own and third-party simulation and optimization tools. Whereas the research effort on the modeling and simulation of processes for aggressively scaled devices has since the foundation of the institute been the core of the activities of the department, in recent years the activities of the department have been strongly extended into the area of "More than Moore", which consists of fields such as analog / RF, low-power electronics, power electronics, and microsystems technology. These new fields of application in particular often require the combination of heterogeneous competencies, because thermal, mechanical, optical, and chemical effects also occur in addition to electronic effects. This gives rise to an additional demand for research.

The department also continues to make important contributions to support the further scaling of advanced nanoelectronic devices. These activities have been mainly carried out in four cooperative projects on the European level, funded either by the European Commission or by the member states: The EU Horizon 2020 project "Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node" (SUPERAID7) coordinated by the department deals with the simulation of the impact of process variations on advanced transistors and circuits. SUPERAID7 started at the beginning of 2016 as a follow-up project of the FP7 project SUPERTHEME which was successfully completed at the end of 2015. More information is given in a separate article below. The traditionally optics-driven resolution improvements through extreme ultraviolet (EUV) lithography have been addressed in the ECSEL KET pilot lines "Seven Nanometer Technology" (SENATE – finished in March 2018) and "Technology Advances and Key Enablers for 5 nm" (TAKE5). The main objective of the the new ECSEL project "Technology Advances for Pilot line of Enhanced Semiconductors for 3 nm" (TAPES3), started in October 2018, is to discover, develop and demonstrate lithographic, metrology, EUV mask technology, devices and process modules enabling 3 nm node technology. These key lithography projects are carried out by large consortia of companies, research institutes, and universities, coordinated by ASML, the leading vendor of lithography steppers. For each of them, the German part is coordinated by Zeiss. The department

SIMULATION

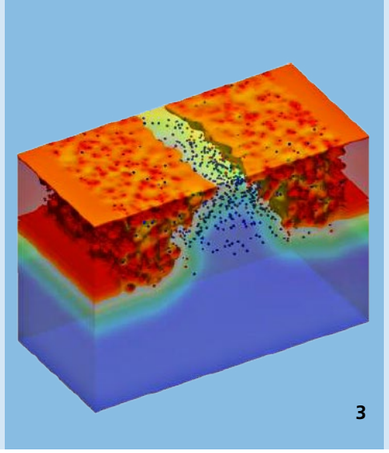
Impact of Process Variations on Advanced Nanoelectronic Devces and Circuits: The H2020 Project SUPERAID7

contributes with the extension and especially with the application of its leading-edge lithography simulator Dr.LiTHO. Furthermore, the department also earns license fees for software developed within “More Moore” projects. Our solid expertise gained in the field of “More Moore”, for instance regarding tailored numerical methods for model implementation, provides a sound basis for the development and application of simulation in other fields, such as “More than Moore”. Lithography simulation is used not only for the development of advanced lithography technology but also for metrology and inspection.

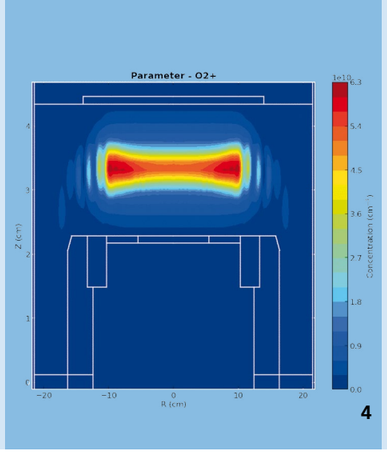
Software engineering techniques are provided and applied in other areas of the institute, among others for smart battery management, which is an important area in power electronics. Genetic algorithms, neural networks and hierarchical modeling approaches are utilized for component and system optimization. Multiphysics simulations that include electrical, mechanical, and/or thermal effects on a case-by-case basis are employed for applications especially in the power electronics area. Methods based on Artificial Intelligence have been increasingly used to enhance traditional approaches for modeling, simulation, and optimization, especially on system level. Key information hidden in large data sets including signals and pictures can be extracted in a largely automated and parallelized way to describe and optimize systems at all levels. The challenge and approach is not to replace physics-based modeling and simulation by data science based predictions, but to combine and utilize the strengths of these two complementary approaches. In order to highlight this approach and mission, towards the end of 2018 the department Simulation has been renamed to “Modeling and Artificial Intelligence”. In order to implement and exploit this approach especially for the optimization of power electronic systems, a new group “AI-Augmented Simulation” has been founded by the end of 2018.

In both the areas of “More Moore” and “More than Moore”, the expertise gained or expanded in publically funded cooperative projects also provides the foundation for several research and development projects directly commissioned and financed by industry, e.g., for the optimization of lithography masks, the simulation of platinum diffusion for power devices, or inductive coupling.

The department will continue its approach to performing focused work on physical models and algorithms in order to develop the necessary skills and tools on the one hand and to transfer these results to applications in industry on the other. Here, a close and trustful cooperation based on sharing work according to the individual competencies and requirements of the partners has been a key element of the success achieved for many years.



3



4

IMPACT OF PROCESS VARIATIONS ON ADVANCED NANOELECTRONIC DEVICES AND CIRCUITS: THE H2020 PROJECT SUPERAID7

Simulation of processes, devices, and circuits significantly contributes to the reduction of costs and time for the development of new technologies and devices in the field of micro- and nanoelectronics. Within the European project SUPERAID7, the project partners developed and applied simulation tools aiming at investigating the influence of process variations. These simulation modules allow one to minimize the impact of variations on devices and circuits.

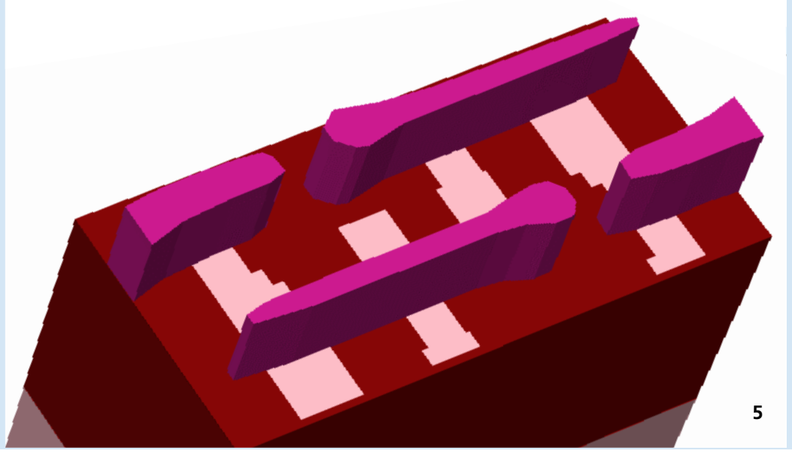
Statistical and systematic variations

Aggressively scaled transistors are affected by two kinds of process variations. Most frequently and long since discussed in the literature are statistical process variations which are caused by the granularity of matter, such as random dopant fluctuations (RDF, see Figure 3): For example, in case of a standard threshold voltage adjustment implant with a dose of $5*10^{12}$ cm^{-2}, at average 2 ions are implanted into a transistor channel of 20 nm length and width. As ion implantation is a statistical process, this means that the actual number of ions implanted into the transistor channel differs from device to device, in that case critically affecting threshold voltage (the voltage at which a transistor switches between on and off state) and other electrical parameters. This is an example for statistical process variations resulting from the granularity of matter for aggressively scaled devices, and was one of the key reasons which ruled out bulk transistors with doped channels for advanced technology nodes.

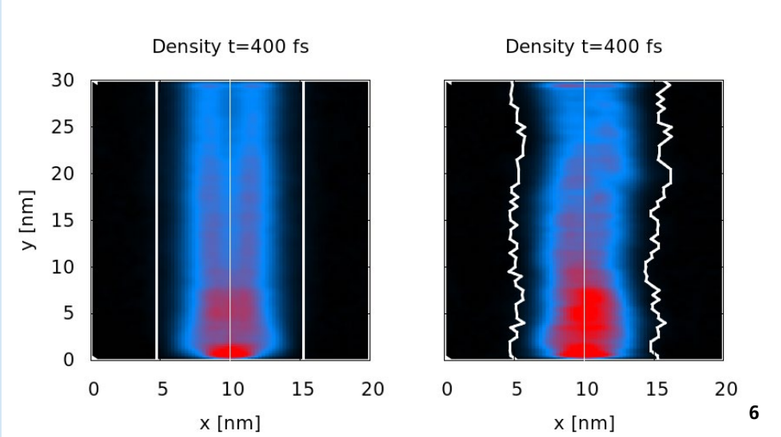
However, especially for three-dimensional nanoscale transistors, the details of the geometries generated during device fabrication are important both for the nominal device performance and for its stability against variations. Other than for statistical variations which can be simulated with stand-alone statistical device simulation, there is a huge variety of potential systematic variations, which must be addressed with various equipment simulation tools and process simulation modules. This includes among others the inherent inhomogeneity of species concentrations (see Figure 4 for an example) or temperature distributions in process equipment, or the variations of equipment parameters which cannot be precisely controlled, such as the distance between the last imaging lens and the wafer in case of optical lithography, the so-called defocus. Moreover, layout effects caused e.g. by pattern density also affect the results of various process steps.

3 *Example for stochastic process variations in a CMOS transistor: random dopant fluctuation (RDF). © Glasgow University sds*

4 *Equipment simulation of a PECVD (plasma-enhanced chemical vapor deposition) reactor. The spatial distribution of the concentration of O_2^+ ions is represented by the color map. The white lines in the figure denote the geometry of the reactor, showing the showerhead electrode at the top and the wafer carrier platen in the middle. For the simulation, a rotationally symmetric geometry has been assumed, a cross section of which is shown in the figure.*



5



6

In turn, it is indispensable for optimized device and circuit manufacturing to well identify and characterize the sources of systematic variability, to sort out those with the largest impact, depending on the device and circuit in question, and to quantify their joint effect on the final nanoelectronic product. The impacts of systematic and statistical variability must be simulated and minimized in parallel, by adapting process flows, but potentially also device architectures and even fabrication equipment.

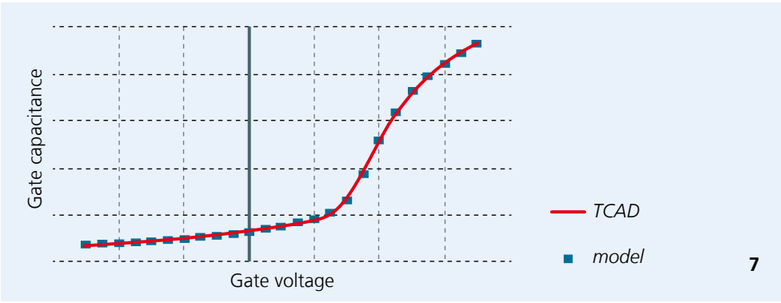
Development of advanced simulation tools to study the impact of variations

In order to meet these requirements, in the cooperative project SUPERAID7 ("Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm node"), a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices was developed. SUPERAID7 was funded from January 2016 to December 2018 by the European Commission within the Horizon 2020 programme . Besides enhanced and new software tools, improved physical models and extended compact models were implemented. In terms of software integration and application, SUPERAID7 was partly based on the SENTAURUS simulation system from Synopsys.

Geometries and their variations are particularly important for aggressively scaled three-dimensional devices as addressed in SUPERAID7. In consequence, the development of an advanced integrated topography simulation tool (see Figure 5 for an example) based on background modules from IISB for the simulation of lithography (Dr.LiTHO), deposition (DEP3D) and etching (ANETCH) and the level-set based topography simulator ViennaTS from TU Wien was a key activity of the project. Besides this, in order to cope with the challenges imposed by very small device sizes and by variations such as surface roughness, improved physical models for confined carrier transport in nanowires (see Figure 6 for an example) are required. These were developed by the partners CEA/Leti, Glasgow University, Synopsys and TU Wien, and integrated into the variability-aware device simulator GARAND of Gold Standard Simulations (GSS), which is since May 2016 part of Synopsys.

Variation-aware compact models for devices and interconnects

Furthermore, variation-aware compact models for highly three-dimensional devices such as stacked nanowires had to be developed. This included three main tasks: First, a novel compact model (LETI-NSP) from CEA/Leti was extended to meet the requirements of SUPERAID7 (see Figure 7 for an example). Second, interconnect compact models were extracted for RC equivalent circuits. Third, a methodology was developed to extend the compact models to include the impact of process variations. The compact model extraction strategy consists of three steps: First, a comprehensive compact model is extracted for the nominal device. Second, a response surface process variation model using a minimum set of parameters is extracted to describe the dependence of process result parameters which define the device, e.g. gate length and width, on the systematic process variations. This extraction is based on the results of the TCAD process simulations carried out. Third, the statistical compact model is generated using corresponding process corners and a second, different set of model parameters. Within SUPERAID7, this compact model extraction strategy has been further enhanced to allow for the direct inclusion of varying equipment parameters (e.g. defocus) instead of or in addition to variations of process result parameters (e.g. channel length).



7

5 *Result of a coupled simulation of lithography and etching for the fabrication of polysilicon gate electrodes (violet) for an SRAM memory structure. Other materials: dark red = oxide, light pink = silicon.*

6 *Simulated electron density (arbitrary units) in ideal (left) and rough (right) nanowire transistors. Red: high density, blue: low density.*
© TU Wien

7 *Comparison between numerical simulations (blue symbols) and compact model simulations (red line) for the dependence of the gate capacitance on the gate voltage for a MOSFET composed of three vertically stacked nanosheets (NS).*
© CEA / Leti

Conclusions

SUPERAID7 very actively disseminated its results to the scientific community, among others via participation in several top-level conferences, organization of three public workshops, and especially more than 40 Open Access publications (see www.superaid7.eu for the download links). Results are being used at all partners to contribute to the further development of semiconductor technologies, devices, or related simulation tools. Especially, results from SUPERAID7 have strongly contributed to the development of Design-Technology Co-Optimization (DTCO) flows at the project partner Synopsys, and to subsequent deployment in the semiconductor industry in Europe and around the world. Variability-aware DTCO is an essential tool to support industry in their efforts to optimize the stability of their products against all kinds of process variations.

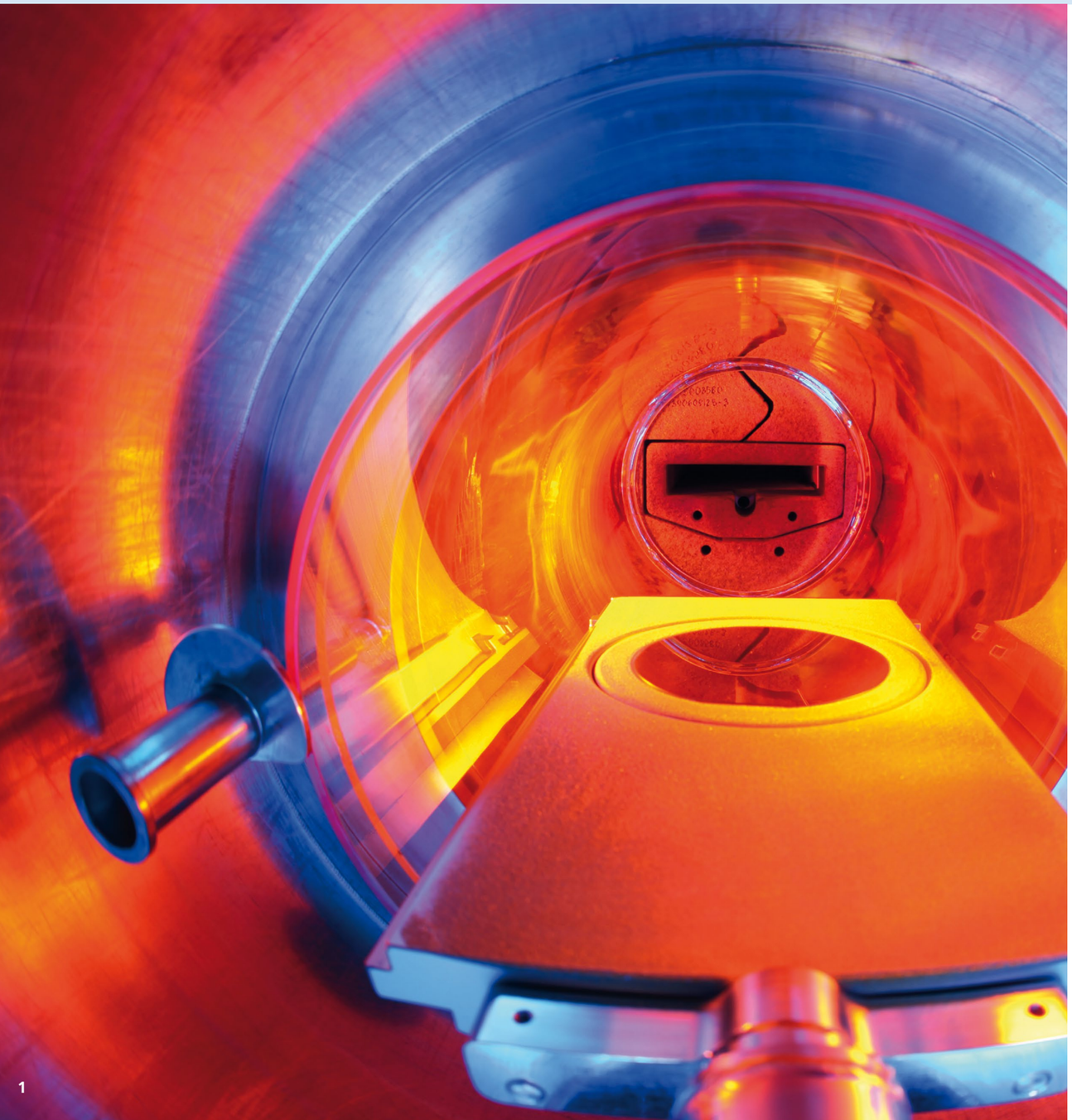
Further information: www.superaid7.eu

Contact

Dr. Jürgen Lorenz
Phone: +49 (0) 9131 761-210
juergen.lorenz@iisb.fraunhofer.de

MATERIALS

2



1

We provide scientific and technological solutions for the development and characterization of semiconductor materials and their production processes.

Our driving motivation is to enable novel applications through the commercialization of these materials. Special emphasis is placed on silicon and wide bandgap semiconductors (SiC, GaN, AlN) for electronic applications, energy saving, and optical systems. The main aim is to support material, device, and equipment manufacturers and their suppliers in the areas of crystal growth and epitaxy. Our materials are further processed into devices and integrated in system demonstrators in-house or at partner sites. To be close to our customers, we operate our branch lab, the Fraunhofer Technology Center for Semiconductor Materials (THM), in Freiberg / Saxony, Germany. The investigation of the relationship between the microstructure of the semiconductor material and the performance and reliability of a respective device gives us the best input for the further development of the materials and their production processes.

The strategy of IISB is a combinatory approach composed of thorough experimental process analysis, tailored characterization techniques, and numerical modeling. These efforts are supported by a well suited infrastructure consisting of R&D-type furnaces, epitaxial reactors, other thin film technologies, state-of-the-art metrology tools for the investigation of physical, chemical, electrical, and structural properties of materials, as well as powerful and user-friendly simulation programs. These programs are especially suitable for heat and mass-transport calculations in high-temperature equipment with complex geometry.

The Materials department gains its competences from an interdisciplinary team of materials scientists, physicists, chemists, as well as electrical, mechanical, chemical, and computer engineers. We have extensive expertise in the areas of crystal growth, epitaxy, thin film deposition, and the synthesis of functional materials including characterization and modeling. Multiple national and international research awards underscore the scientific and technological achievements of the Materials department. These awards have been granted for outstanding scientific and technological results, as well as for excellent contributions to the education of students and engineers. In collaboration with the University of Erlangen-Nürnberg, the Technical University Georg-Simon-Ohm Nuremberg, and the Technical University Bergakademie Freiberg, the Materials department supervises students carrying out research projects, including bachelor, master, and PhD theses.

In 2018, the majority of research topics at the Materials department were in the areas of silicon, silicon carbide, gallium nitride, and aluminum nitride.

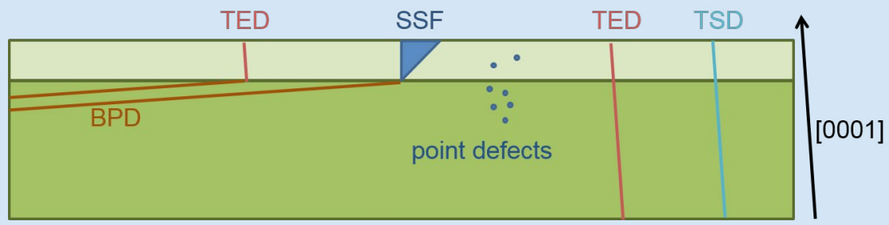
In the field of directional solidification of silicon for photovoltaic applications, we have developed a numerical model which is able to identify the contamination paths of metallic impurities in the crucible – coating – melt – crystal system depending on different parameters such as crucible

1 *View into horizontal hot-wall reactor for SiC homoepitaxy during wafer loading.*
© K. Fuchs / Fraunhofer IISB

2 *Dr. Jochen Friedrich, head of the Materials department.*
© K. Fuchs / Fraunhofer IISB

MATERIALS

Scrutinising SiC Epilayers



3

size, coating thickness, purity of crucible coating and feedstock. The model delivers valuable quantitative insights into the physical processes and helps to reduce further the contamination of the silicon ingot with metallic impurities.

In the field of Czochralski grown silicon, we used numerical modeling to support our industrial partner in the development of the next generation of pullers. By optimization the hot zone of the puller we were able to increase the productivity of the next generation puller by more than 50 %. In addition a non-destructive technique was developed to measure the geometry of the so-called growth ridges of Czochralski and Floating Zone grown silicon crystals. This allows to obtain quantitative information about the thermal field which acts during growth and to correlate it with the properties of the as-grown crystals.

In the field of nitride semiconductors, we had put into operation the so-called wafering laboratory which was funded within the German FMD initiative. With the investment we are now able to process GaN and AlN crystals into wafers with functionalized epi-ready surfaces. These wafers are further processed in house or at partners' site to test devices to proof the wafer quality. In addition we had identified by different analytical methods, that the presence of so-called V-pits during epitaxial growth of AlGaN / GaN heterostructures on silicon will affect the breakdown voltage. The cause is the growth kinetics, which differs within the V-pit leading to a higher incorporation of impurities. This leads to a local reduction of the electrical resistivity and subsequently to a reduced breakdown voltage.

In the field of silicon carbide, we continued our analysis of extended and point defects in the substrate and the epilayer. In this regard new metrology tools which were funded by the German FMD initiative were put into operation. The x-ray topography (XRT) tool gives the possibility to investigate crystallographic defects such as the amount and different types of dislocations, slip lines, dislocation networks, (small angle) grain boundaries, inclusions, precipitates, pits, scratches, etc. with high speed and high resolution on full wafer scale on bare wafers, wafers with epilayers, partially processed wafers as well as bonded wafers. The XRT is an ideal supplement to the new defect scanner which combines an optical surface and photoluminescence imaging system and which allows also the measurement of several extended defects in SiC with very high spatial resolution.

SCRUTINISING SiC EPILAYERS

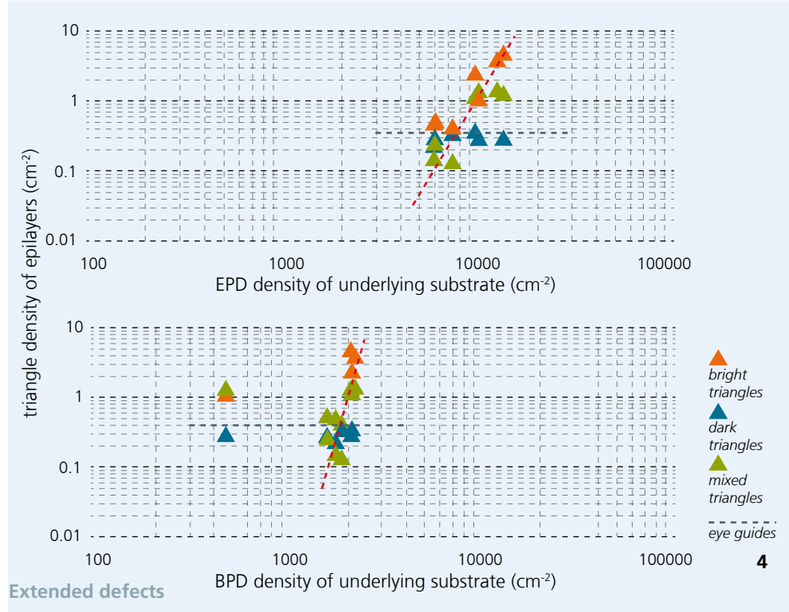
Careful control of the growth process limits the carbon vacancies that govern the carrier lifetimes, but some extended defects and point defects in epilayers are determined by the substrate quality.

Lying at the very heart of every SiC power device is a stack of homoepitaxial layers. Each of them has a carefully selected doping concentration profile and thickness, because this determines the key characteristics of the chip: its blocking capability and its on-resistance.

Unfortunately, these homoepitaxial layers can inherit many forms of extended defects from the substrate, including dislocations and stacking faults, which may hamper device yield and reduce reliability. So how do variations in substrate quality influence the epilayers? And can the substrate quality also influence the point defect concentration, and ultimately the carrier lifetime of homoepitaxial layers and devices?

Working on the answers to these important questions, and related issues, is our team from Fraunhofer IISB, MOCVD manufacturer Aixtron, and Intego, a producer of metrology equipment. Using 100 mm and 150 mm diameter 4H-SiC substrates from a variety of vendors, we have grown SiC epilayers by CVD and scrutinised the resulting material. This work sheds new light on concerns over wafer quality that are common within the SiC industry – many of those that work within it know that there is a specific defect signature for each vendor, associated with the densities and lateral distributions of dislocations and stacking faults.

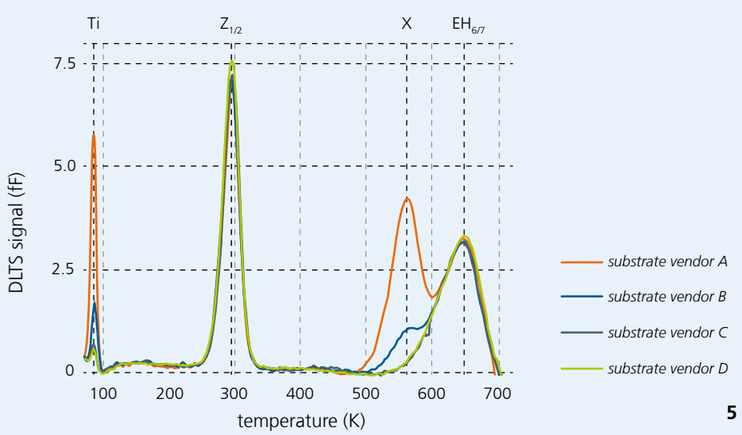
3 *SiC substrates and epiwafers contain many forms of defects, including point defects, stacking faults (Shockley stacking fault, SSF), and various types of dislocations, including: the basal plane dislocation, BPD; the threading edge dislocation, TED; and the threading screw dislocation, TSDs.*



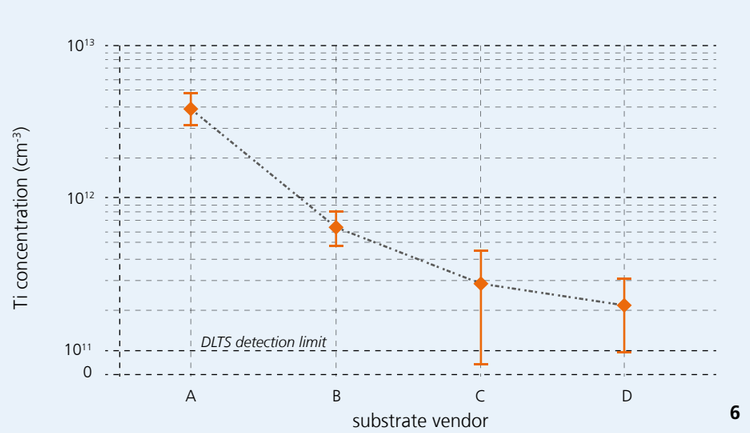
4

Extended defects

4 *The densities of triangular-shaped stacking faults ("triangles") in 4H-SiC epilayers and the dislocation densities in the underlying substrates. The triangle densities of epilayers were determined with ultraviolet photoluminescence imaging, while the dislocation densities of underlying substrates were interpolated from defect selectively etched reference wafers.*



5



6

Common dislocations in SiC substrates include threading edge or screw dislocations, which lie nearly perpendicular to the surface (along the [0001] c-axis); and basal plane dislocations, which are orientated almost parallel to the wafer surface on the c-plane (compare Figure 3).

During epilayer growth, the threading dislocations in the substrate tend to make their way into the epilayer. Some threading screw dislocations convert to Frank-type stacking faults, and some to stacking fault complexes like carrots and comets. Fortunately, engineers don't have to worry about these threading dislocations in the epilayers, as they are harmless in most forms of power electronic device. Stacking faults, however, are a major concern, as they impair device performance and reliability.

The most notorious defect is the basal plane dislocation. It can propagate into the epilayer, where it is transformed into a Shockley-type stacking fault or a threading edge dislocation. The former is a menace, causing severe degradation in bipolar devices. Due to this, great strides can be made by uncovering the origins of the stacking faults in these epilayers, and devising appropriate ways and means to minimize their presence.

Motivated by this goal, we have recently turned our attention to comparing the density of triangularshaped stacking faults in epilayers with the density of dislocations in the underlying substrates. To do this, we have exposed these stacking faults with ultra-violet photoluminescence imaging. This technique produces images with darker and brighter triangles than their background, and features triangular defects with both bright and dark regions – so-called mixed triangles. By inspecting these images, we can see that the triangular shape of the stacking faults in the epilayers originates from the off-axis growth and the hexagonal symmetry of 4H-SiC. We have also undertaken defectselective etching of reference wafers, to determine the dislocation densities of the underlying substrates (see Figure 4).

The densities of the bright and mixed triangular defects appear to be related to the dislocation density of the substrate. This implies that these triangular defects originate from either basal plane dislocations or threading screw dislocations in the substrate. However, for dark triangles, their density is independent of the dislocation densities in the substrate. That's because the dark triangles originate from ingrown particles, which can be controlled in the epitaxial growth process.

There is still more work to do. Our plan is to undertake a further, more detailed investigation of the densities and the origin of extended defects in epilayers, using a pair of new lab tools: an X-ray topography tool XRT Micron from Rigaku, and an ultra-violet photoluminescence imaging system from Intego, equipped with surface inspection. Armed with the insights these instruments will bring, we aim to identify the critical defects for high-quality, reliable devices. This should lead to guidelines for acceptable defect densities for substrates on one hand and for optimum epitaxial growth parameters on the other hand.

Point defects

When a process engineer dials in the growth temperature, gas flows and pressures, as well as influencing the impact of extended defects, their choices determine the doping concentration and thickness of the epilayers, as well as homogeneities across the wafer.

Using a modern reactor, the Aixtron G5WW, we can produce epilayers with very good doping homogeneities and a wafer-to-wafer reproducibility of less than ± 6 percent. Even more impressive results, however, are realised with Aixtron's AutoSat technology. On 150 mm wafers, this addition reduces the wafer-to-wafer temperature uniformity from ± 3 K to just ± 0.5 K. This drops the wafer-to-wafer doping deviation to less than ± 3 percent, which is an excellent result for an 8 x 150 mm production reactor.

The extremely homogeneous, reproducible temperature distribution that occurs in our epitaxial growth chamber enables some of the intrinsic point defects in the epilayers to be controlled very well, as they are generated thermodynamically. Take, for example, the carbon vacancy. It exerts the greatest influence on the carrier lifetime in n-type epilayers, and its abundance is determined by two factors: the extent of carbon excess, and the temperature during epitaxial growth.

To gain insight into the point defects in n-type epilayers, we have investigated epilayers grown under identical conditions, on substrates from four different vendors. We probe all these layers, grown under conditions that ensure the same temperature, carbonto-silicon ratio, and doping concentration, using deeplevel transient spectroscopy. This technique uncovers four distinct peaks, including two associated with a carbon vacancy.

For the carbon vacancy known as $Z_{1/2}$, the concentration is very reproducible (see Figure 5). It is independent of the substrate used and has a level of 5 x 10^{12} cm^{-3}. Other groups have also studied this vacancy, and their reports indicate that our level is very competitive. Note that we have found that the concentration of the carbon vacancy can be controlled by epitaxial growth conditions.

The titanium defect is present in all epilayers grown under identical growth conditions, but its concentration varies by a factor of 25, from 2 x 10^{11} cm^{-3} to 5 x 10^{12} cm^{-3} (see Figure 6). Its defect level is governed by the make of the substrate.

5 *Deep-level transient spectroscopy has been used to probe epilayers grown on substrates from different vendors under identical epigrowth conditions. All the epilayers contain the titanium (Ti) defect and carbon vacancies (represented by $Z_{1/2}$ and $EH_{6/7}$). The X defect occurs only in epilayers grown on substrates from vendors A and B.*

6 *Data obtained from deep-level transient spectroscopy of epitaxial wafers from four growth runs shows that the titanium concentration at the top of the pilayers depends on the vendors of the substrates. Data points represent mean values, while error bars define the minimum and maximum values.*

MATERIALS

Scrutinising SiC Epilayers

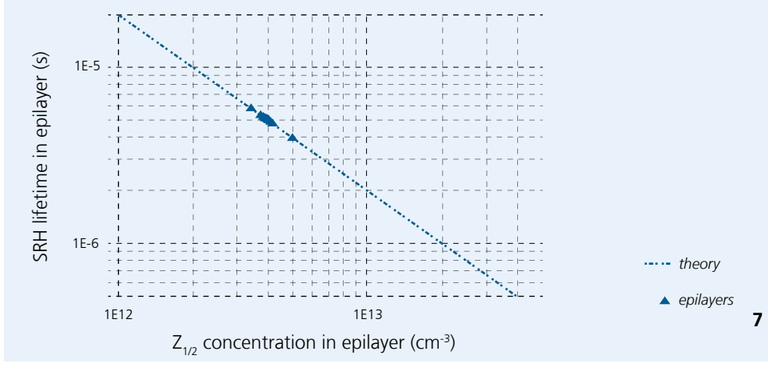
We have also studied the influence of epigrowth conditions, such as the carbon-to-silicon ratio and the temperature, on the concentration of titanium in epilayers grown on substrates supplied by one vendor. This investigation reveals that the levels of titanium are not related to the conditions during the epigrowth process or the reactor hardware. We are still investigating the mechanism for the transfer of titanium from the substrate to the epilayer.

Deep-level transient spectroscopy also uncovered a defect that is found only in the epilayers grown on substrates provided by two of the four vendors. We are yet to determine the nature and origin of this defect, labelled X, but we plan further investigations.

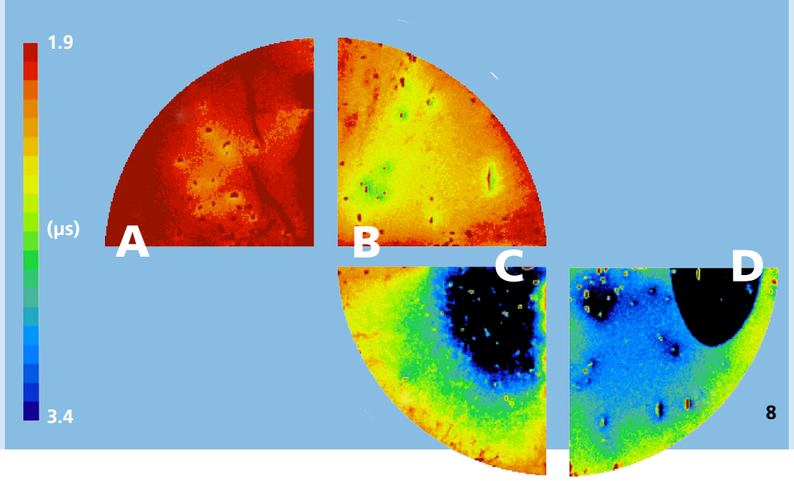
Carrier lifetimes

Another insight provided by deep level transient spectroscopy is that the concentration of all point defects in the n-type epilayers is, compared to the typical doping, lower by two-to-three orders of magnitude. This verifies the high quality associated with the epitaxial growth processes and the hardware.

Point defects influence the carrier lifetime in the epilayers, and can ultimately govern device performance. For example, the carbon vacancy is a known lifetime killer, and its impact on the carrier lifetime can be predicted with Shockley-Read-Hall statistics. With typical growth conditions, the concentration of the carbon vacancy varies from 1 x 10^{12} cm^{-3} to 3 x 10^{13} cm^{-3} – depending on the growth temperature and the carbon supply – and this produces variations in the carrier lifetimes from longer than 10 µs to less than 1 µs (see Figure 7). For our epilayers, the lifetime is about 5 µs, a competitive value.

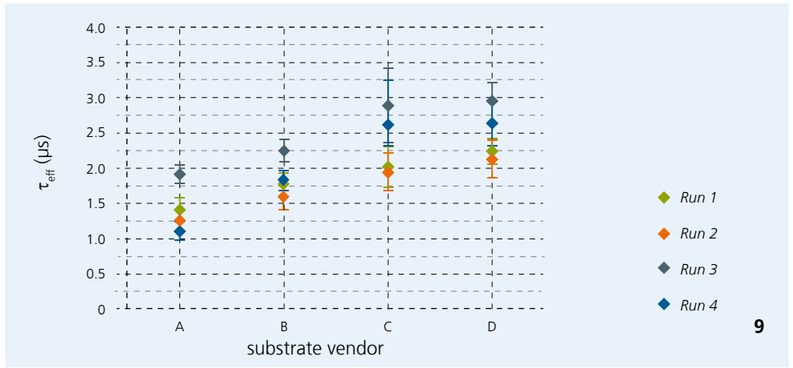


7



The most common method for determining carrier lifetime is the microwave-detected photoconductivity decay. This method yields a value for the lifetime that depends on the Shockley-Read-Hall lifetime of the epilayer itself, but also contains contributions related to surface recombination and interface effects between the epilayer and the substrate. The value for this effective lifetime is always less than that for the Shockley-Read-Hall lifetime of the epilayer.

We have measured the carrier lifetimes on 16 epiwafers These are taken from four runs, each containing one substrate from each of the four vendors. The results show significant differences in lifetime, dependent on the source of the substrate (see Figure 8 and 9). We are still to uncover the reason for this.



9

Our efforts show that today's multi-wafer reactors are capable of providing excellent homogeneities and reproducibility with regard to temperature, epiwafer thickness and doping uniformity. This enables engineers to control intrinsic point defects, such as the carbon vacancy. However, the control of some extended defects, or some influences on the effective lifetime are governed by the substrate.

7 *The Shockley-Read-Hall (SRH) lifetime as a function of the carbon vacancy concentration, calculated for microwave-detected photoconductivity decay measurement conditions (line) and individual epilayers. The $Z_{1/2}$ concentration obtained from deep-level transient spectroscopy provides values used for the carbon vacancy concentration.*

8 *Effective lifetimes of 65 µm-thick, low n-doped epilayers obtained from microwave-detected photoconductivity decay, exemplary set of wafer quarters. Note in wafer quarter 'D' the presence of extended defects as small regions with a lower lifetime and the wafer facet.*

9 *Effective lifetimes of 16 wafer quarters from four epigrowth runs.*

Contact

Dr. Jochen Friedrich
Phone: +49 (0) 9131 761-270
jochen.friedrich@iisb.fraunhofer.de

TECHNOLOGY AND MANUFACTURING

2

1

Technology and manufacturing at Fraunhofer IISB mean above all research, development, and prototype manufacturing in the field of power electronic devices on silicon (Si) as well as on 4H-silicon carbide (SiC). In particular to meet the requirements of our external and internal customers better, the service sector is set up in a separate organizational unit called π-Fab. π-Fab is intended for the fabrication of custom-tailored prototype electron devices, mainly for power electronic application, and it is ISO 9001:2015 certificated for this.

For this purpose, IISB and the Chair of Electron Devices of the University of Erlangen-Nuremberg operate joint clean room facilities of 1500 m² (primarily class 10) with CMOS-compatible equipment. This allows the implementation of important process steps on silicon wafers with diameters of up to 200 mm and on SiC wafers with diameters of up to 150 mm. An industrial CMOS process transferred to IISB and constantly adapted for research and development purposes is used as a reference and as the basis for developing advanced process technologies. The main activities focus on the fields of Si power semiconductors, passives, and silicon carbide electronics. IISB has increased its commitment especially to SiC by implementing new equipment and processes to meet special and additional requirements for SiC power device processing. Most of the FMD investments of the Technology and Manufacturing department are dedicated to the change in wafer size on SiC from 100 mm to 150 mm. This above all concerns the etching and refilling of deep trenches and the high-temperature processing of SiC. Furthermore, the FMD investment allows us to broaden our process portfolio by providing backside grinding and polishing for SiC wafer thinning and providing laser annealing for backside ohmic contact formation of already on the front side processed wafers. As a result, industrially competitive low ohmic contact can be provided. All of this allows the department to strengthen its competence in manufacturing high-voltage power devices. By now, IISB has developed its resources and expertise to the point where it can perform nearly all manufacturing steps on SiC substrates according to an industrial standard. The devices currently under development include diodes and merged pin diodes in the voltage ranges from 1.2 kV up to 4.5 kV, as well as MOSFET devices such as vertical or lateral DMOS. A trench technology for vertical diodes and MOSFET as well as sensor and high-temperature CMOS devices are in progress.

For the development of novel process steps in the field of dielectrics and metallization, IISB operates advanced sputter and chemical vapor deposition tools on the basis of ALD that are used for the deposition of high-k and metallic layers. Furthermore, special activities focus on ion implantation technologies. At IISB, implantation tools with acceleration voltages ranging from a few eV up to 800 keV are available. Special implantations for CMOS as well as for power semi-conductors have been established (for example, commercial tools have been modified to be able to implant several wafer diameters and manifold elements at elevated temperatures).

1 *Line for SiC-wafer backside processing.*
© K. Fuchs / Fraunhofer IISB

2 *Dr. Anton Bauer, head of the Technology and Manufacturing department.*
© K. Fuchs / Fraunhofer IISB

TECHNOLOGY AND MANUFACTURING

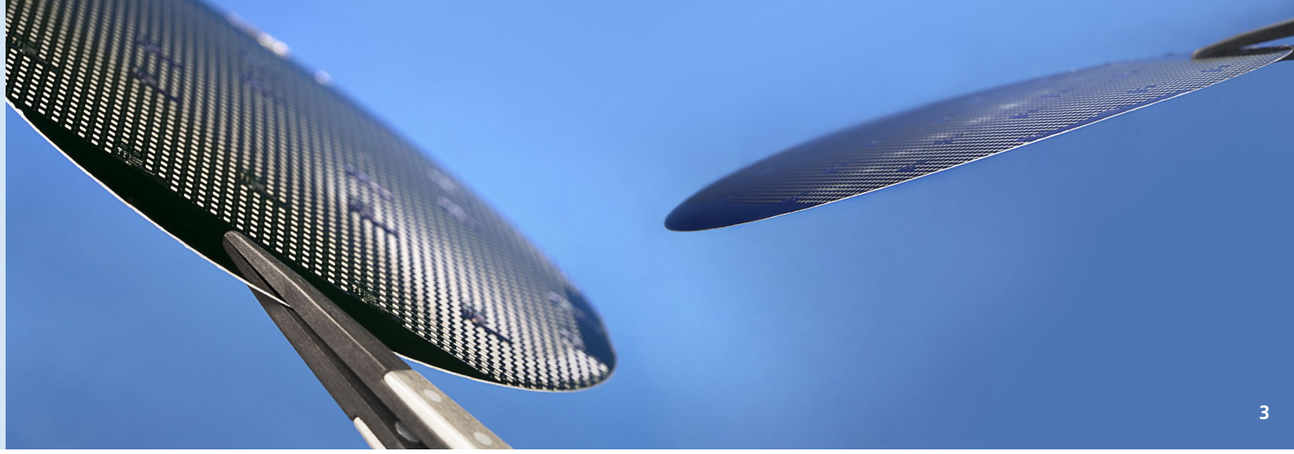
New Back Side Processing to enhance ON-Resistance of SiC Power Devices

The physical and electrical characterization of process steps and device structures is of the utmost importance for the manufacturing of semiconductor devices. Important steps in this respect are the determination of the topography, doping profile, and further physical and chemical parameters, as well as FIB investigations, energy-dispersive X-ray analysis, and AFM surface characterization of layers. A specific competence of the department is the combination of several methods for failure analysis during the processing of semiconductor devices and tracing the causes of failure. The spectrum for electrical characterization has been further increased (e.g., lifetime measurements and high-voltage measurements especially for SiC).

Furthermore, from nanotechnology to printable macro-electronics, the Technology and Manufacturing department is your contact for the realization and characterization of single process steps up to prototype devices. Based on comprehensive clean-room facilities, further activities are becoming more and more relevant. An example of such current activities is low-temperature deposition of inorganic materials using printing techniques. The emerging markets for such products are control units and specific sensors based on inorganic materials. The field of thin-film systems ranges from materials to device exploration to the development of TOLAE (thin, organic, and large-area electronics) applications. Based on a carefully targeted selection from solution processing/printing, spray coating, or vapor deposition of inorganic layers, the devices are optimized for their respective environment. Printed electrolyte sensors integrated with read-out and data handling electronics allow physical strain to be monitored in wearable sports trackers and can also be utilized in the chemical industry, water quality assessment, or several agricultural tasks. Capacitive and temperature sensing in combination with high performance TFTs enable the realization of smart integrated thin-film systems.

Another focal area of the department's work is the processing of structures in the range of a few nanometers as well as the repair and analysis of electronic device prototypes by means of focused ion beam (FIB) techniques and electron beams. In addition to that, UV nano-imprint lithography, a cost-effective fabrication technique that allows the transfer of nano-sized features to photoresist without the use of advanced optical lithography by applying small rigid stamps and, most importantly, by applying large-area (up to 150 mm) flexible stamps too, is now well established.

The IISB analysis laboratory for micro- and nanotechnology with various chemical, physical-chemical, and physical test methods is essential for a conclusive and comprehensible assessment. Two working groups at Fraunhofer IISB contribute their expertise in advanced process control, manufacturing science, productivity, contamination control, and yield control aspects to the ENIAC project "EPPL", which aims to combine research, development, and innovation to demonstrate the market readiness of power semiconductor devices fabricated in leading European 300 mm pilot lines.



3 *Processed SiC device wafer with 90 µm total thickness.*

NEW BACK SIDE PROCESSING TO ENHANCE ON-RESISTANCE OF SiC POWER DEVICES

Owing to its physical properties, silicon carbide (4H-SiC) is a key material to fabricate low ON-resistance semiconductor devices which are of utmost importance power electronics and therefore for significant energy saving. Clearly, in a 4H-SiC power device (e.g. a Schottky diode) there are several contributions to the total ON-resistance (R_{ON}) as drift layer, SiC substrate and contact metallization. Due to the much lower ON-resistance of SiC drift layers compared to Si, SiC is well suited for power devices blocking 600 – 1200 V. But, there is still a noticeable resistivity contribution from the SiC substrate itself, which has no electrical function. For example, in a 650V SiC Schottky diode fabricated onto a 350 µm thick substrate about 70 % of the total R_{ON} is represented by the SiC substrate

As a consequence the SiC substrate should be removed to the largest possible extend without endangering the functionality or the manufacturing yield of the devices. To minimize the risk of wafer breakage during further processing, the number of process steps after the grinding should be kept as small as possible. Therefore the backside wafer grinding is performed on front side finished devices. To stabilize the wafer during grinding, backside ohmic contact formation and solder stack deposition as well as to avoid imprints on the wafer backside caused by large (up to 12 µm in height) 3D-structures on the front at the grinding step, the wafer is temporary bonded with a specific glue to a glass substrate for the a above mentioned processing steps. Another challenge is the backside ohmic contact formation, which needs a comparatively large thermal budget (typically ~ 980 °C for 5 min). This can't be performed with the standard thermal budget used for the front side, because it would significantly influence the electrical performance of the part of the device on the front side. Therefore it's necessary to alloy the backside metallization by laser to avoid any thermal load on the front side.

In 2018, as part of FMD (Forschungsfabrik Mikroelektronik Deutschland) project, Fraunhofer IISB implemented all significant tools for backend of line fabrication processing of SiC power devices, consisting of a tool park for temporary bonding, grinding and polishing as well as laser annealing for ohmic contact formation.

The backend of line processing was successfully applied to 2nd Gen. SiC JBS diodes, which were developed and manufactured in-house. Following sequence has been performed. At the beginning the SiC wafer with the front side finished devices was spin coated front face with a specific thermoplastic adhesive film which is highly suitable to level high 3D structures common for power devices as passivation layers. To give off solvents the coated wafer was baked out on

TECHNOLOGY AND MANUFACTURING

New Back Side Processing to enhance ON-Resistance of SiC Power Devices
Towards a Digital Twin for Fraunhofer IISB's Prototype Fabrication of Electron Devices

4

a hotplate before it was temporary bonded front face on a glass carrier wafer. Afterwards the bonded SiC device wafer was grinded to the final target thickness. The grinding step consists of a rough grinding to reduce wafer thickness rapid and a fine grinding step to reduce mechanical stress on the wafer caused by the rough grinding step. Then the ohmic metal was deposited on the wafer backside, which has to be alloyed to form a decent low ohmic contact. Therefore the metal layer on the device wafer's back was annealed by a UV laser before the solder stack deposition. Subsequently the temporary bond was dissolved by a thermo-mechanical debonding system. At the end the thinned device wafer was cleaned of adhesive residuals by solvents.

In this way, the wafer thickness could be reduced to a total thickness of 90 µm, of which the substrate thickness is around only 65 µm as can be seen in Figure 3. By laser annealing the backside contact resistance could be obvious reduced and the uniformity could be distinctly improved compared to lamp thermal annealing. All in all, caused by the new back end of line processing at Fraunhofer IISB the ON-resistance could be lowered to 90 mΩ of the 650 V Schottky-diode, which means a reduction of more than 30 %.

TOWARDS A DIGITAL TWIN FOR FRAUNHOFER IISB'S PROTOTYPE FABRICATION OF ELECTRON DEVICES

Motivation: Flexibility as a Matter of Principle – and a Source of Challenges

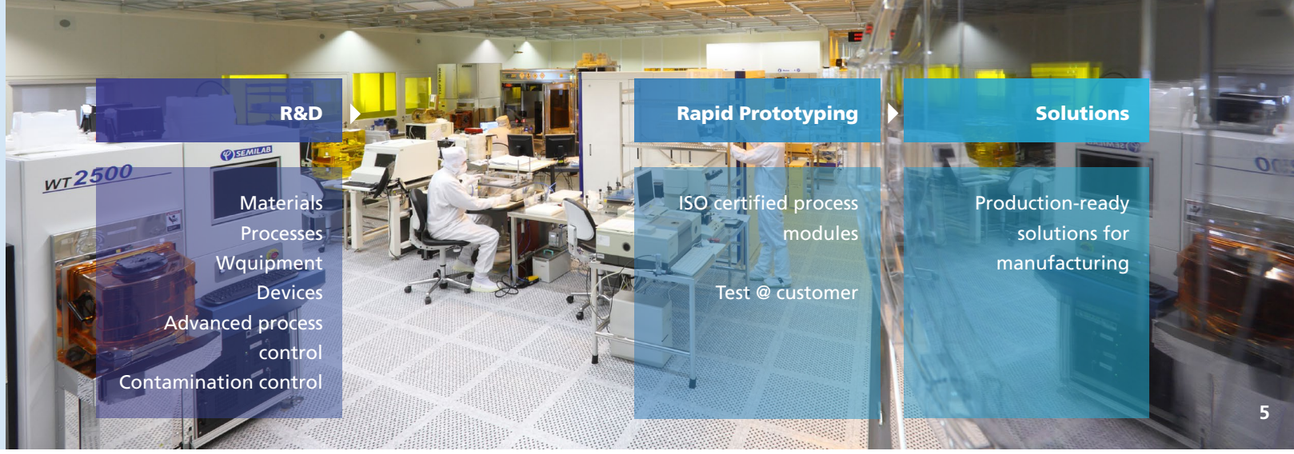
The Fraunhofer IISB runs the π-Fab (see Figure 5), which comprises a continuous silicon CMOS process chain in an industry-compatible environment, where a silicon carbide process line is integrated. Here, prototyping services for electron devices (i.e., power devices, CMOS devices, passives, sensors, and MEMS) and processes are offered and performed (details: www.iisb.fraunhofer.de/p-fab).

The main challenge for such a prototyping line is to address a multitude of customer requirements in a flexible manner, e.g., with regard to material, device layout, or functionality. While most custom designs build and rely on a proven and optimized set of process steps, it is the mere nature of "prototyping" to replace or augment existing process steps with novel or modified ones, which are tailored to the respective customer's needs. This requires the smart combination of a certified library of proven process or device modules with results from "on the fly" research and development. As every production site with high product diversity and low volume per product, the π-Fab faces the challenge of an every-changing product-specific knowledge base.

4 *The digital twin of Fraunhofer IISB's π-Fab collects data, extracts information from it, and turns the obtained information into knowledge and actions.*
© Fraunhofer IIS / IISB

TECHNOLOGY AND MANUFACTURING

Towards a Digital Twin for Fraunhofer IISB's Prototype Fabrication of Electron Devices



5

The question is how to effectively learn and act in such a flexible and volatile environment to achieve best quality and repeatability for the customers.

R&D Approach: Elaborating a Digital Twin

To answer this question, Fraunhofer IISB carries out focused development within the European project iDev4.0 ("integrated Development 4.0") to evolve its π-Fab towards a smart platform for rapid prototyping. The research approach is to elaborate and implement a "digital twin", i.e. a digital duplication of the π-Fab (see Figure 4). The digital twin can then be used to collect and store data and information from the real world, learn from it, and turn the results into knowledge and actions for the real world again (for more information on a digital twin, see Figure 6).

The first version of the "π-Fab digital twin" will focus on smart experiments for accelerated process transfer and flexible concepts for manufacturing control, tailored to a rapid prototyping environment. Respective results will be used to augment existing π-Fab elements in a smart manner to enable new perspectives for the prototype fabrication of smallest lot-size with high product diversity on different substrate materials.

Smart Experiments

In the flexible prototyping environment of the π-Fab with a high mix of products, lowest product volumes, and both R&D and production evolving in parallel in the same manufacturing line, an efficient use of every available bit of information and data is essential to quickly transfer latest R&D results into certified prototyping. To achieve this objective, we started research on the novel concept of "smart experiments". So far, two important steps were taken:

1. A group of experts from the equipment, process, and data analytics domains identified in a joint effort the most challenging processes that require accelerated process transfer. As a result, the focus will be on an etch cluster, comprising three chambers dedicated to specific etching steps.
2. In parallel, a concept for smart experiments was developed. Figure 7 summarizes the initial concept, while the alignment of the approach with the other project partners is ongoing.

By applying this approach, a quick identification of a high-quality and comprehensive set of experiments is aimed at, thus allowing a decrease of design and learning cycle time to be reached in prototyping. The first concept evaluation and validation approach considering dry etch processes will show, whether the aspired 20 % reduction of integration-time for newly developed processes becomes possible.

Principal aspects of a digital twin:

- A digital twin is a digital representation of the real world, comprising e.g. models and algorithms to mimic the real behaviour
- A digital twin collects, stores and summarizes data available from the real world environment
- Within a digital twin, and based on its inherent models and collected data, data analytics and methods of artificial intelligence can reveal complex correlations, predict process changes or equipment fails, and support playing through what-if scenarios
- A digital twin reflects the results back to the real world to optimize processes, enhance quality, speedup process development, etc.

6

5 *Fraunhofer IISB's π-Fab covers R&D and ISO-certified rapid prototyping of semiconductor devices. Customers may transfer results from rapid prototyping to mass manufacturing at other production sites.*

6 *The principal aspects of a digital twin.*

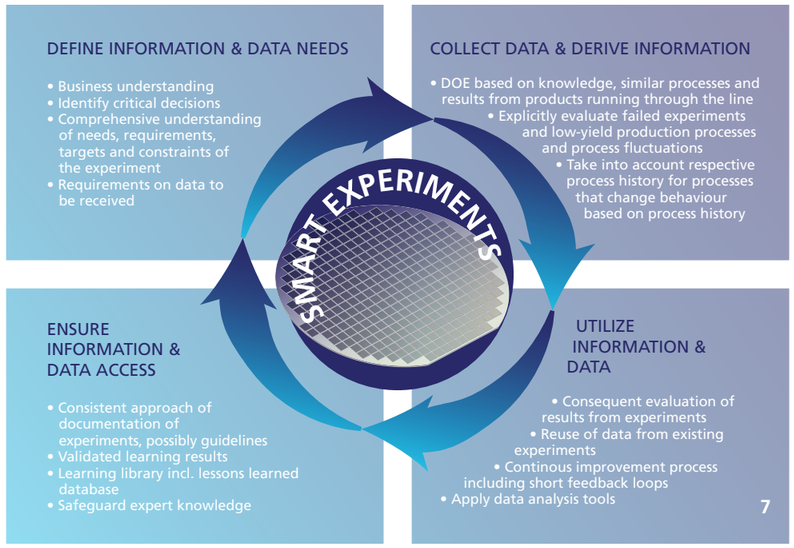
Smart Logistics and Advanced Contamination Control

For high-quality and reliable products it is usual in industrial high volume production to use only precisely defined processes and to monitor the processes closely with the use of various software systems, e. g., a manufacturing execution system (MES). This is a distinct difference to Fraunhofer IISB's prototype fabrication of electron devices, where a multitude of customer requirements with regard to material, device layout, or functionality is being addressed in the process chain. This flexibility is a matter of principle and leads to a continuous change of process steps and process flows in the prototype fabrication. In order to optimize the entire value chain, from order to customer and back again for process / device improvements, flexible manufacturing control techniques have to be developed and utilized.

Fraunhofer IISB is working within iDev4.0 on smart logistics and flexible manufacturing control concepts for rapid prototyping. Functionalities and requirements for adaptive process flow planning, process execution, and process parameter adjustment based on results of real-time and smart experiments, are currently being defined. The developed concepts will be later implemented during the rollout of a new manufacturing execution system, which takes place as part of the "Research Fab Microelectronics Germany / Forschungsfabrik Mikroelektronik Deutschland" (FMD).

TECHNOLOGY AND MANUFACTURING

Towards a Digital Twin for Fraunhofer IISB's Prototype Fabrication of Electron Devices



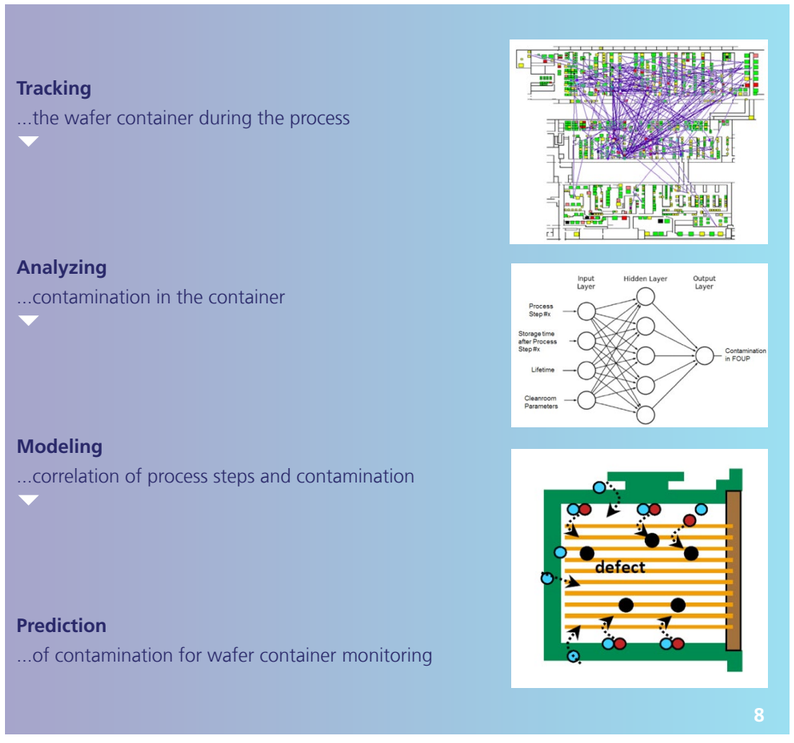
Another important challenge in manufacturing and prototyping, respectively, is the implementation of advanced contamination control procedures. Based on the π-Fab's flexibility, various wafer sizes and types are being handled in different contamination protocol zones and the customer may determine the points of entry and exit from the process line. To overcome this challenge innovative contamination control strategies are currently developed by Fraunhofer IISB utilizing the concept of digital twins.

Figure 8 shows the principle of the intended concept for a digital twin of a wafer container. The tracking information of the wafer and the corresponding wafer container will be combined with the analysis of data from in-line and off-line contamination control procedures to finally model and predict the contamination behavior depending on lot process flow and transportation routes. First investigations have been started with data sets provided by an industrial project partner.

Project Information

The project "integrated Development 4.0" leads the digital transformation of singular processes towards an integrated digital value chain based on the "digital twin" concept. Development, planning and manufacturing will benefit from the "digital twin" concept in terms of highly digitized virtual processes along the whole product lifecycle.

The project iDev4.0 has received funding from the ECSEL Joint Undertaking under grant agreement No 783163. The JU receives support from the European Union's Horizon 2020 research and innovation program. It is co-funded by the consortium members, grants from Austria, Germany, Belgium, Italy, Spain and Romania.



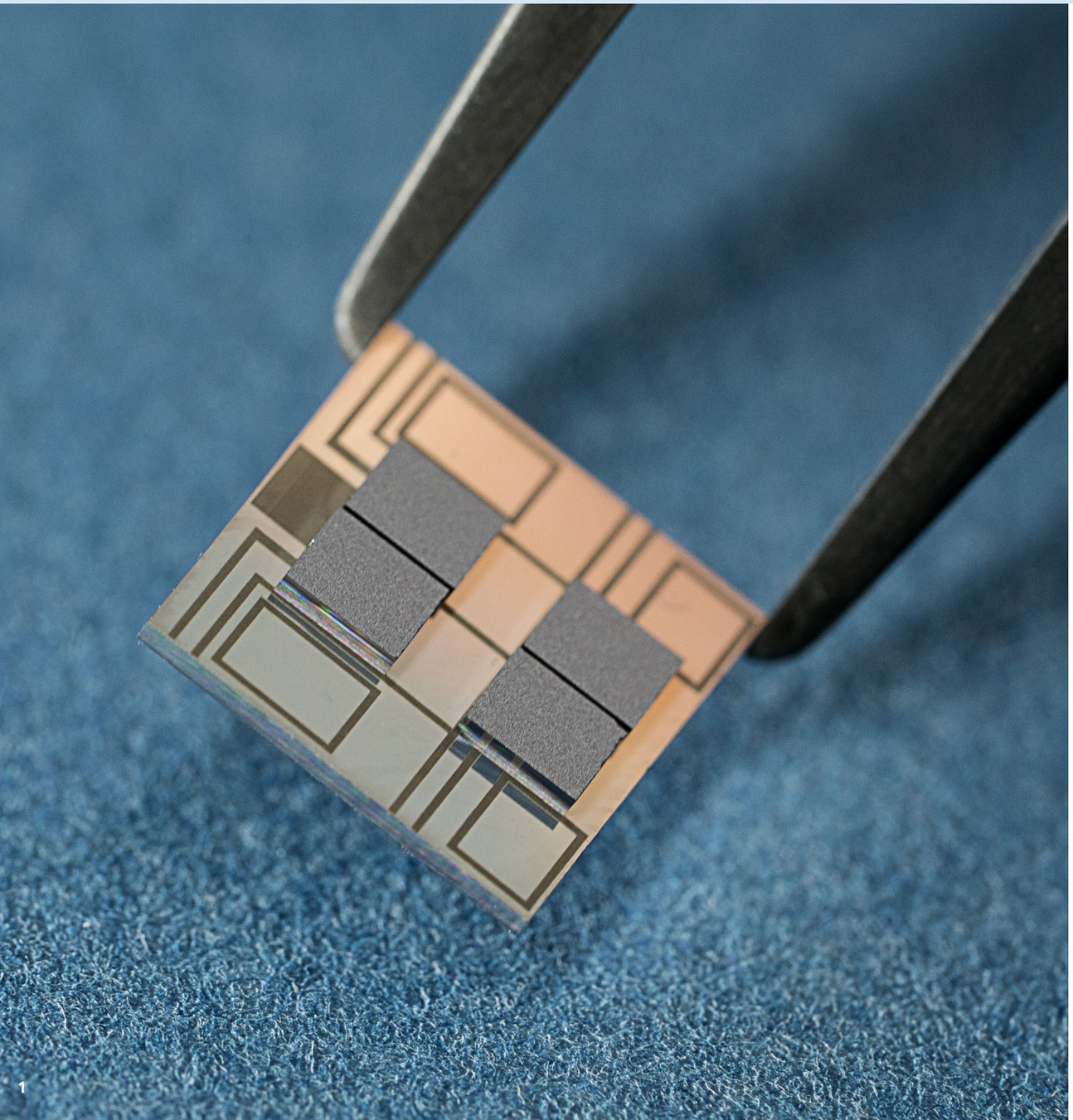
7 *The concept of "smart experiments".*

8 *Digital twin principle for wafer container.*

Contact

Dr. Anton Bauer
Phone: +49 (0) 9131 761-308
anton.bauer@iisb.fraunhofer.de

DEVICES, TEST AND RELIABILITY



1

2

The department acts as a bridge between the Semiconductor Technology business unit, which is focused on materials and processes, and the application-oriented Power Electronics business unit. The fields of research include design and fabrication aspects of active and passive devices, packaging technology and concepts, as well as electrical characterization, lifetime testing, modelling, and reliability.

The development of silicon carbide devices is steadily progressing. In 2018, trench JBS diodes with reduced forward voltage drop (approx. 1.4 V forward voltage drop for 600 V / 5 A devices) were realized by including substrate back-thinning technology.

In the joint collaboration, with the National Institute for Nanomaterials Technology in Pohang, Republic of Korea, Fraunhofer IISB has successfully introduced a baseline VDMOS technology with NINT. The project has passed the first two-year stage accruing the highest rating of all present GRDC projects in Korea. A close collaboration between both institutions and significant exchange of staff was established as the basis for subsequent joint R&D activities in Korea and Germany. Next, Fraunhofer IISB has started its development on 150 mm SiC TrenchMOS technology.

Based on a SiC CMOS baseline technology, high-temperature capable circuits were implemented and device modelling has started. Besides the basic digital and analog circuit functionalities, integrated SiC RESURF LDMOS transistors were realized for the first time in on a SiC CMOS technology platform.

For the monolithic integration of capacitors and snubbers for implementation with fast-switching SiC- or GaN-based power modules, the design of 1200 V capacitors is close before technology transfer to an external silicon foundry service for mass production.

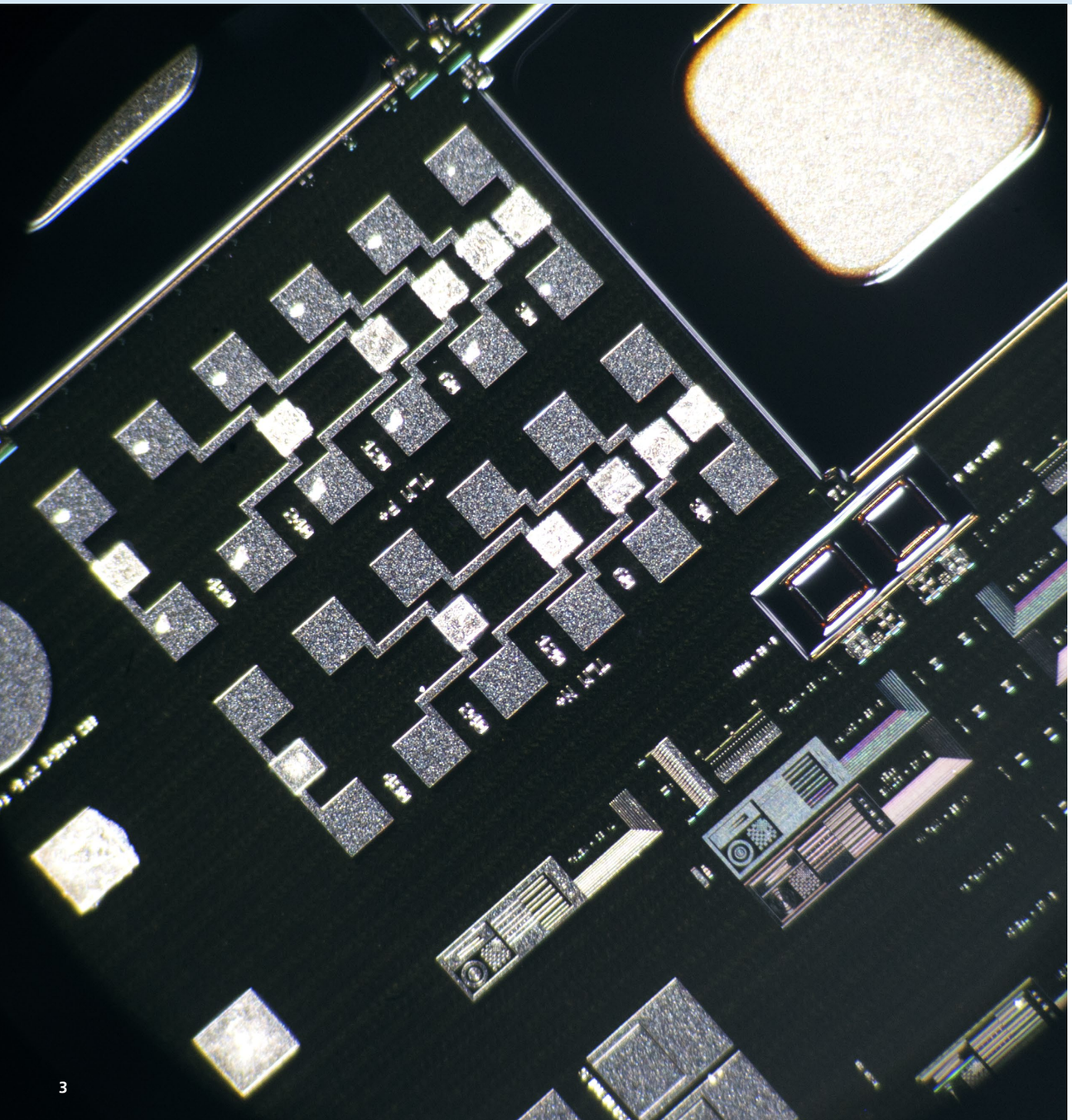
In the field of packaging, new research projects have started. ZuLeSelf, sponsored by the Federal Ministry of Education and Research (BMBF), was kicked off in 2018. The project will support the research area electrochemical corrosion with condition monitoring and modelling.

The successful work of the past was continued, especially on the topic of die attach. In particular a direct bonding technology was developed. Now it is possible to stack semiconductor components without any additional intermediate layer like solder or sinter material. Thermomechanical testing is going on right now in order to show the relevance for power electronics. For silver sintering of semiconductors, a quite promising technology was established. It is the so called selective sintering technique. There it is possible to bond thermally stressed and demanding devices by sintering onto a pre-populated printed circuit board. The result is a mixed packaging technology

1 *Typical application of direct bond: four MOSFETs bonded on a Si-Interposer.*

2 *Andreas Schletz, head of the Devices and Reliability department.*
© K. Fuchs / Fraunhofer IISB

DEVICES, TEST AND RELIABILITY



3

for surface mount devices and power electronics. The test results addressing thermo-mechanic endurance show excellent results.

The new clean room for new packaging concepts and technologies is established. Many tools have been installed and set up. The complete packaging line from storage, printing, die bonding, soldering and sintering, encapsulation, and testing is available in a high-quality packaging lab. Thanks to the ongoing project "Research Fab Microelectronics Germany (FMD)", sponsored by the Federal Ministry of Education and Research, new hardware was installed that allows new research to be well equipped for the future. In 2018 the new paste jet printing machine came into operation. First tools for 3D printing of polymer materials arrived. The packaging group is active in the FMD topic "Heterointegration".

The research activities concerning testing and reliability have moved to a new big "environmental test lab". Most of the equipment is now clustered at one single place resulting in short walking distances and an optimized material and workflow. Thanks to the FMD project, new active and passive temperature cycling tools are set up.

Material characterization for the next generation of lifetime modelling for power electronics is ongoing. Besides the bond line of semiconductor devices, direct bonded copper substrates were in the focus. The complete process chain from material characterization, modelling and simulation was established. The new public funded research project, "SiCool", was kicked off in 2018, and will be supported by the Federal Ministry of Education and Research. The aim is to develop a physics-of-failure-based lifetime model in conjunction with state-of-the art failure in time (FIT) modelling for power and signal electronics located on the same circuit board.

The testing of ceramic capacitors is still in the focus. The devices will play a big role in the future of power electronic filters and DC links thanks to their high energy and power densities and their ability for high-temperature usage. Right now, the group has a good overview on available ceramic capacitors and their lifetime expectations in terms of passive and active application of static and transient high voltages and static temperatures.

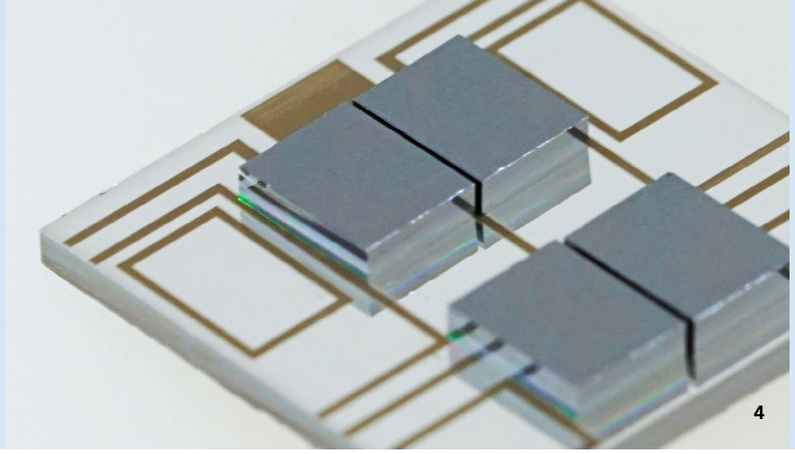
In addition to the variety of public funded projects, there were a huge number of joint industrial projects in all research fields. The topics ranged from assistance and consulting to large feasibility studies and process and technology developments for devices, packaging, and testing. The applied research within the department is financed by an industrial budget contribution of well above forty percent. This perfectly achieves the Fraunhofer target.

Many thanks to all colleagues for their great support during challenging times and the excellent work that has led to success and keeps the institute ready for the future.

3 *6A / 650V JBS-Diodes on completely processed SiC wafer after thinning to a final thickness of 90 µm.*

DEVICES, TEST AND RELIABILITY

Reducing ON-Resistance for SiC JBS Diodes by Thin Wafer Technology
Power Electronics meets Fine Pitch – Direct Bond Technology



4

REDUCING ON-RESISTANCE FOR SiC JBS DIODES BY THIN WAFER TECHNOLOGY

With superior properties like wide bandgap and high critical electrical field strength, silicon carbide (SiC) is a very attractive choice for power semiconductor devices. One of the most common and fundamental devices are Schottky diodes. Key to fulfilling nowadays requirements of high performance, Schottky devices require reduced on-state voltage drop while maintaining low leakage current at high blocking voltages. In their history of development one key approach was to combine Schottky with PiN diodes, bringing together the advantages of both but also resulting in a trade-off between forward and blocking capabilities.

One key item to improve the performance of the SiC diodes is to reduce substrate thickness. The thickness of the epitaxial layer, the electrical relevant layer in SiC power devices, is in the range of a few micrometers, depending on its voltage class. In contrast to that, the substrate onto which the epitaxial layer is grown has a thickness of 350 µm. With that, the device performance benefits from a thinner substrate thickness due to its significantly reduced contribution to the differential resistance, leading to a reduced on-state forward voltage drop while maintaining blocking capabilities.

Constant progress and investments in SiC technology at Fraunhofer IISB are driving the continuous improvement of the manufactured power devices. In 2018, Fraunhofer IISB introduced wafer thinning and laser annealing dedicated to manufacturing of 4H-SiC power devices. Wafer thinning and laser annealing were successfully applied to in-house designed and manufactured 2nd Gen. SiC 5A / 650V JBS diodes with our industry partners. These devices exhibit an on-state voltage drop reduction from 1.68V to 1.52V at rated current while maintaining voltage blocking capabilities of over 1.1 kV and leakage currents < 1 µA at 650 V.

Moreover, established technologies like Al-implantation followed by a high temperature annealing step for dopant activation were used to obtain p^+ grid characteristical to JBS diodes. Based on the knowledge and experience, which is augmented by numerical and analytical device simulations, improvements of the customized p^+ field guard ring design were realized. With moderate leakage currents up to 175 °C, a surge current capability of 90 A, (measured with surge pulse of 8.3 ms) and contact resistance below 300 µΩcm^2, several performance goals have been achieved, making the 4H-SiC diodes competitive to commercial manufactured devices on the market and leading to a small volume fabrication project in the following years.

Further investments in the silicon carbide trench etching capabilities at Fraunhofer IISB are paving the road for a trench JBS manufacturing technology as a major goal for the following years, developed free of third party processing IP.

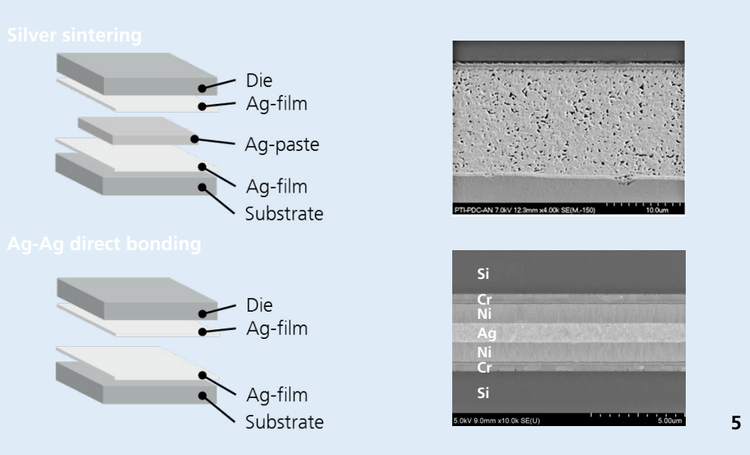
4 *Typical application of direct bond: four MOSFETs bonded on a Si-Interposer.*

5 *Schematic and cross-sectional SEM micrographs of the bonding interface. left: Silver sintering, right: Ag direct bonding.*

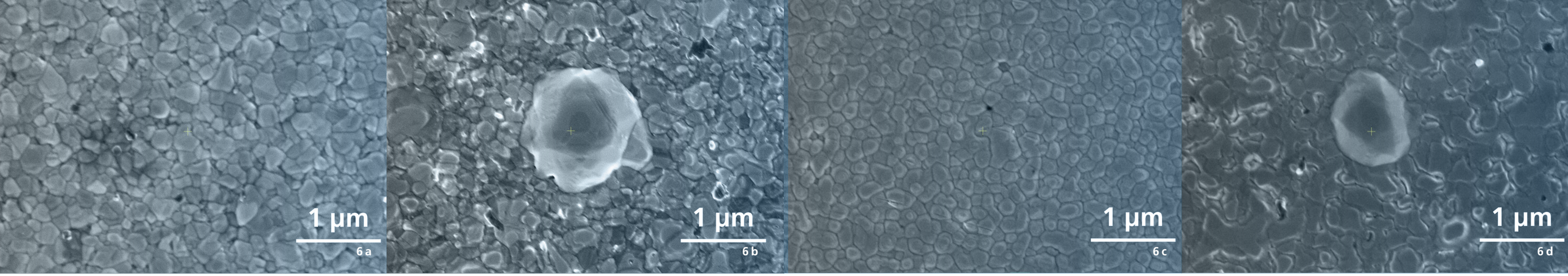
POWER ELECTRONICS MEETS FINE PITCH – DIRECT BOND TECHNOLOGY

Next-generation power devices such as silicon carbide and gallium nitride devices have proven superior switching performance, while being capable of high-voltage and high-temperature operation. Therefore, wafer-level and 3D integration concepts like chip-stacks, through silicon via (TSV) and silicon interposer design, which provide short interconnects with low parasitic effects, are becoming more and more interesting for power electronic applications.

Interconnect and die-attach technologies in 3D power integration are currently limited by ultra-fine pitch devices. Although many other bonding technologies, such as thermo-compression bonding, transient liquid phase bonding and silver sintering are extensively used to replace conventional soldering, relatively high bonding temperature and pressure, as well as complex manufacturing routines processes are required for a homogeneous bonding interface. Therefore, direct bonding has been investigated as an alternative die-attach technique for fine structures.



5



This technology allows joining partners with a thick top side metallization together without an additional intermediate layer.

Mechanism of direct bonding

High-temperature processing of the devices leaves the metallization with a large mechanical stress due to different coefficients of expansion (CTE) of the materials. Therefore, stress migration, which is driven by a stress gradient, often occurs in the metallization. During this diffusion-controlled process, the so-called hillock formation and abnormal grain growth have been observed in the metal films as a result of stress relaxation. The as-deposited film has equiaxed grains with sizes smaller than the film thickness. The small, normal grains may continue to grow but large abnormal grains grow at faster rates. These abnormal grains grow generally by annihilation of surrounding normal grains until they impinge on each other. By using numerous hillocks and abnormal grains on Ag films as bonding medium, high-strength bond lines can be achieved at low temperature and pressure.

Direct Bond Research Activities at Fraunhofer IISB

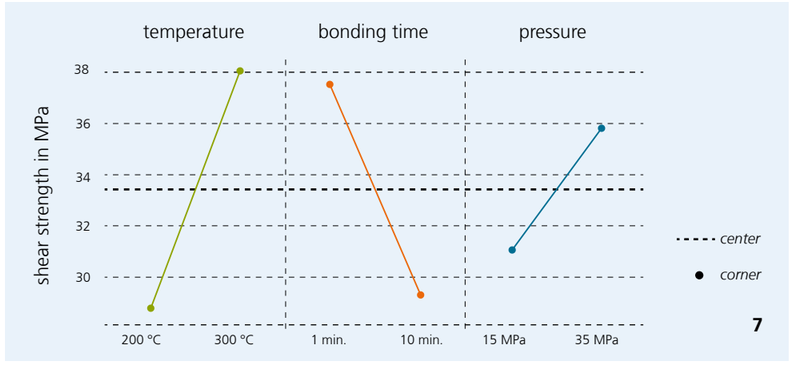
At Fraunhofer IISB, direct bondingwith Ag metallized dies and substrates has been recently researched and analyzed. The effects of various processing parameters such as temperature, bonding time and pressure on shear strength are firstly investigated via the design of experiments (DoE) method. Experiments according to a two-level full factorial design are utilized to determine an optimal parameter set for achieving the maximum shear strength. Based on the results of DoE, the highest shear strength of 50 MPa could be achieved with Cr/Ni/Ag metallized samples by bonding at a temperature of 300 °C for 1 min with an applied pressure of 35 MPa.

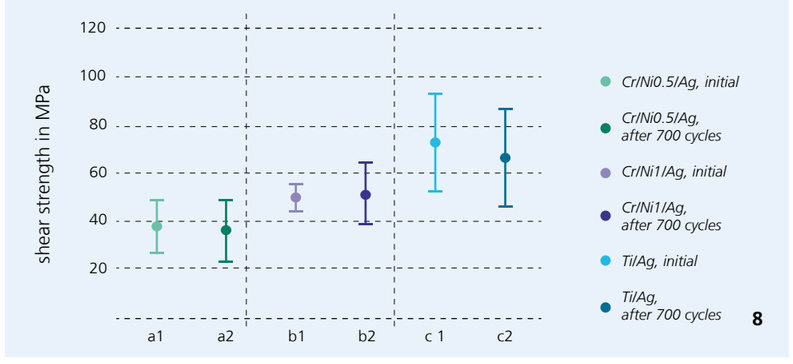
Further, the surface morphology evolution of the Ag films was investigated to understand the mechanisms of the stress migration bonding. Fine and uniform grains were observed in all the as-deposited Ag films. Compared to the as-sputtered Ti/Ag films, Cr/Ni/Ag films have a larger grain size. According to previous results, hillock formation is more likely to occur at a higher temperature than 250 °C. An apparent hillock growth was observed in all Ag film surfaces after a thermal treatment at 300 °C for 1 hour. As the temperature increased to 350 °C, the number of hillocks was significantly increased. In addition, large grains are observed in the Ag film surrounding the hillocks, however, accompanied by numerous voids.

Further, a heating time over 60 min at 300 °C can also lead to large void formation. Compared to the Cr/Ni/Ag metallized samples, highly increased shear strength of 73 MPa can be achieved with Ti/Ag film.

To determine the resistance of the Ag direct bonds to alternating temperature extremes, temperature cycling test (TCT) was carried out in a two-chamber thermal shock setup (+150 °C / -55 °C; 15 min / 15 min). Three test groups, each with a different metallization were cycled to compare the lifetime of the direct bonds. All the samples were bonded using the same optimized parameters (300 °C, 35 MPa, 1 min). Scanning acoustic microscopy (SAM) was used to characterize the samples during TCT to identify voids and delamination in the silver joints. Moreover shear tests were carried out on the samples before and after TCT to measure the ageing of the bonding strength of Ag joints. Additionally, neither delamination by SAM nor decrease in shear strength was detected for direct bonded samples after 700 thermal cycles.

In summary, with the suitable film stacks and process parameters, high-strength and long lifetime stable Ag direct bonding can be achieved. This interconnection technology looks very promising for next-generation power semiconductors.





6 *SEM micrographs of the microstructures in the Ag films,*
a) as-deposited Cr/Ni/Ag film,
b) Cr/Ni/Ag film after annealing,
c) as-deposited Ti/Ag film,
d) Ti/Ag film after annealing.

7 *Main effect diagram for temperature, bonding time and pressure for direct bonding of Cr/Ni/Ag metallized Si dies.*

8 *Die shear strengths of Ag joints before and after TCT.*

DEVICES, TEST AND RELIABILITY

Lifetime of advanced Multilayer Ceramic Capacitors (MLCC)

9 *Electrical fail of a capacitor leads to macroscopic damage of the device visible as crater of a micro-explosion. The impact of this failure to a system increases with the energy stored in its capacitors.*

LIFETIME OF ADVANCED MULTILAYER CERAMIC CAPACITORS (MLCC)

MLCCs find their way into more and more applications – including automotive traction – leveraging on their compact outline and current carrying performance. This increasing market penetration especially into demanding technologies is fueled by the development of advanced materials such as ferroelectric or anti-ferroelectric dielectrica, which allow the manufactures to enhance the relative dielectric contant er and thus increase the capacitance of a device at a given volume.

This volumetric efficiency resp. capacitance density of the modern MLCCs, enable further system miniaturization and high density designs. Furthermore, the ceramic materials sustain a wide minimum and maximum temperature range allowing their use in harsh environments. Also their maximum DC operation voltages enable higher voltage designs.

Looking to the electric characteristics, high power and high frequency designs benefit from their low loss dielectrics and low ESR electrodes reducing ohmic losses as well as small form factors reducing inductive parasitics.

Except for their todays high price, the advanced MLCC devices look perfect for advanced high density systems.

Being deeply involved into power electronic system development, it is natural that we are going beyond the datasheets and are taking a closer look on performance, lifetime and physics of failure of these modern devices:

Looking to literature, there are a number of studies on lifetime of ceramic capacitors; however mostly focusing on leakage currents in static aging tests, mostly on ferroeletric / X7R types and mostly at voltages below 100 V. We extend the experimental reach to in-situ leakage current and capacitance measurement of MLCC, such as modern NP0 / COG and anti-ferroelectric types, with passive and active heating from room temperature to up to 200 °C and with bias voltages up to 2000 V at a statistically significant sample size down to pico-Ampere and pico-Farads. This allows us to study the stability of capacitance over temperature, voltage and time as well as lifetime of leading edge devices such as latest antiferroelectric or COG capacitors at their point of operation, e.g., 500 V and beyond.

Applying operation voltages or temperatures beyond the specification limits is a well-established aging method for the highly acceleration of lifetime test (HALT) and described, e.g., by the Prokopowicz and Vaskas (PV) equation. During the static test a constant bias voltage V is applied to the devices under test (DUTs) being exposed to a controlled environment e.g. constant, but elevated temperature T. In order to accelerate aging this bias voltage V typically exceeds the specified maximal operation temperature V_0 gaining an acceleration i.e. shortening of lifetime by a factor of $(V_0 / V)^n$ with the voltage stress exponential n, which depends on the type of capacitor under test; the elevated temperature T also shortens the lifetime proportional to a Boltzmann-factor $\exp(E_a / k_b (1 / T - 1 / T_0))$ with E_a denoting the activation energy for the temperature dependent contributions with typical values of 1 eV to 2 eV for most capacitors and k_B denoting the Boltzmann constant.

The extraction of these acceleration parameters and test recommendation for specific devices is supported by advanced failure analytics and modelling of their physics. This is the focus of the ongoing investigation.

Given the fact that MLCCapacitors are more and more used e.g. also by massive parallel integration as DC-Link at high voltages and elevated operation temperatures we strive to understand and predict a failure of a single capacitor and its impact on the complete system.

Contact

Andreas Schletz
Phone: +49 (0) 9131 761-187
andreas.schletz@iisb.fraunhofer.de

VEHICLE ELECTRONICS

1

2

Vehicle Electronics – much more than inverters for electric cars!

The Vehicle Electronic Department keeps on working on new, compact power electronic solutions for mechatronic integrated drive inverters, high power DC/DC converters, and new solutions for charging system. The improvements of SiC and GaN power semiconductors are paving the way to much compacter and more efficient solutions. They can be integrated more easily into electric motors or battery system and are a key to future mechatronic integrated solutions for next generations on electric vehicles. This further integration of power electronics will reduce size, weight, and costs for the electric power train of electric passenger cars.

Beside this publicly discussed electrification of passenger cars, there is an upcoming request on electrification solutions for commercial vehicles to reduce the CO_2 and noise emissions as well as the operation costs. The first electrified public transport busses are already operated in the big cities and new electrified construction vehicles and trucks will come soon. Because of the high and continuous power demand of such applications they cannot be supplied by battery systems. The vehicle electronic department is developing new DC/DC converters to connect fuel cells or overhead lines to the electric power train to realize very long operation times.

The starting research on electric air mobility brings complete new challenges for power electronic solutions in case of light weight and fail operation design. The IISB is tackling these challenges by advanced circuit design using most advanced active and passive components and a high level of mechatronic integration. A great example for this approached is the air cooled SiC inverter integrated in the nose cone of an electric propulsion system developed in the EU funded research project “Autodrive”.

The new fail operational concepts for power electronic converters and power supplies are also important for future autonomous vehicles. The sensors, actors, and the control logic have to be fail operational to fulfill the safety requirements. New solutions for a failure tolerant power supply are developed in the public funded BMBF project “HiBord”.

To keep up with the growing demand of advanced power electronic solutions the Vehicle Electronic Department is continuously growing, with now 55 engineers and technicians. To tackle the high power demand of construction vehicles trains and the future aircraft propulsion systems in the megawatt range, the medium voltage group was affiliated to the vehicle electronic department.

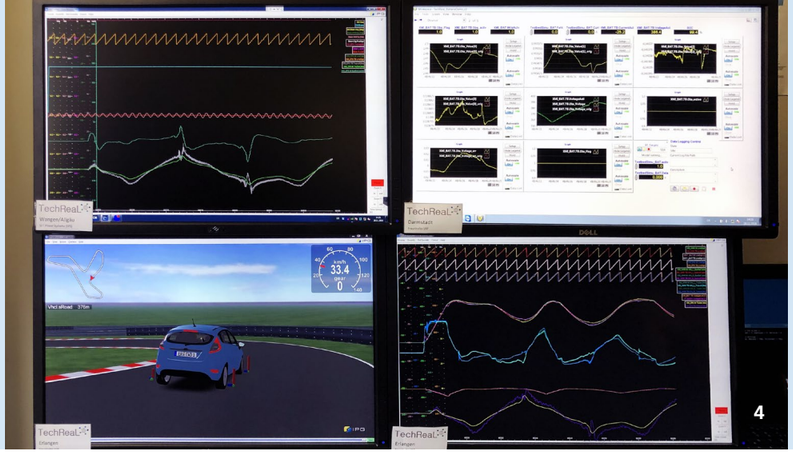
A great thank to all our partners for the assigned projects and funding as well as to all colleagues for their eager work and excellent results.

1 *Medium Voltage Test Lab at Fraunhofer IISB for the Characterization of Medium Voltage Power Electronic Systems up to 30 kV and 20 MVA for Mobility, Energy, and Aviation.*

2 *Dr. Bernd Eckardt, head of the Vehicle Electronics department.*
© K. Fuchs / Fraunhofer IISB

VEHICLE ELECTRONICS

Connected Testing of Electric Powertrains



CONNECTED TESTING OF ELECTRIC POWERTRAINS

Global trends including environmental legislation, electrification, automation, and reduced time-to-market affect all mobility industries and require more agile development processes. In the vehicle industry, the shift from internal combustion engines to partly or fully electric drive trains creates new degrees of freedom with respect to the number and combination of motors, engines, batteries, fuel cells, etc. When taking into account battery charging, advanced lateral and longitudinal control, advanced driver assistance functions, and automated driving, the complexity of possible system configurations increases even further. Therefore, efficient test procedures are required to ensure performance, functionality, interoperation, functionality, reliability, and product safety of the vehicle system.

Established Methods

Currently, simulating the overall vehicle functionality and testing real components on dedicated test beds are established practices. Exchanging high level software models between supplier and system integrator is relatively easy, but modelling complex nonlinear system behavior proves difficult. Component test beds are usually available on-site at the component supplier's or at dedicated service providers, but can only test components and not systems.

Complete system functionality of vehicles is defined by the complex interactions between different components provided by different suppliers. To test the system behavior, integrating the components with each other is a mandatory step. The existing approaches to integration include the construction of test vehicles and the use of complete system test benches. Both approaches have major disadvantages:

Test vehicles require relatively high effort to construct, and all components need a certain level of system and integration readiness. Component specialists' presence on site is often difficult to organize, measurement equipment available in the vehicle or on-site is limited, test sites must be booked, equipment and vehicles must be moved, and travelling to the test site is time consuming for the specialists. If problems occur during testing, these difficulties even increase.

Test time at complete test benches is expensive and the test benches are quite inflexible, especially if a great variety of, e.g., drivetrain architectures must be covered. While high-class test equipment may be available at such sites, the issues regarding the assembly of different companies' experts on-site prevail.

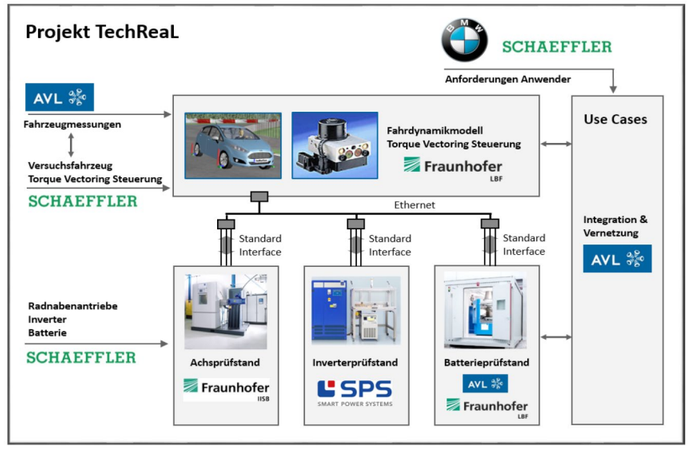
3 *Two Schaeffler E-Wheel-Drive wheel hub drives on Fraunhofer IISB's connected axle motor test bench.*

4 *Simulated vehicle on virtual test track and measurement data of components on the connected HiL test beds at Wangen / Allgaeu, Darmstadt and Erlangen.*

VEHICLE ELECTRONICS

Connected Testing of Electric Powertrains

5



6

Connected Testing

During the BMBF (German Federal Ministry of Education and Research) funded project 'TechReaL', a different approach was investigated:

Instead of bringing all components together for integration in a vehicle or at a complete system test bench, the components remain at the test benches which are used during component development. These component test benches are connected to a distributed hardware-in-the-loop (HiL) test bench in real-time via internet connections. A central complete vehicle model serves as a virtual integration platform, where all components are integrated. The vehicle model processes sensor data from the test benches. The model sends back set-values to the test benches' actuators and communicates with the components under test.

In 'TechReaL', two Schaeffler E-Wheel Drive wheel hub motors were mounted on a drive axle test bench at the Fraunhofer IISB E-Mobility Test Center. A high voltage traction battery, a drive inverter and an electric power steering actuator where located at project partners' sites in Germany and Austria.

The virtual vehicle model calculated wheel speeds based on the dynamic running conditions of the vehicle and sent torque requests to the wheel hub motors. The actual torque was measured and fed back into the vehicle model. Also, the DC supply voltage of the motors was dynamically set by the vehicle model, based on the actual voltage of the real HV battery at the remote battery test bench. The interconnection of the test benches was realized with an encrypted virtual private network, which connected the test benches and components to the central virtual vehicle model. The test bench operators, test engineers and component specialists communicated via internet and telephone conferences, screen sharing, and webcams. Upcoming issues with components could be fixed by the local experts within short time and the system tests could be resumed quickly.

The project evaluation showed the great potential of this approach. It enables early integration tests which allow for shorter feedback loops and fosters a development process which can react on integration related issues more agile than established methods. It can thus help gaining a better system understanding and higher overall system quality faster, earlier, and at lower cost.

Contact

Dr. Bernd Eckardt
Phone: +49 (0) 9131 761-139
bernd.eckardt@iisb.fraunhofer.de

5 *The TechReaL network connects locations in Germany and Austria.*

6 *Project overview with illustration of the connections between the HiL test benches and with the virtual test vehicle.*
© TechReal

INTELLIGENT ENERGY SYSTEMS

1

2

The department "Intelligent Energy Systems" develops the technologies for the digitalization of the power electronic and energy conversion in the transportation and energy domains. The department integrates these technologies in interconnected intelligent energy systems, building the "Cognitive Power Electronics" ecosystem initiated by Prof. Lothar Frey at the Fraunhofer IISB. Its research and development efforts are focusing on cutting-edge power and control electronic hardware, as well as on software and data processing technologies making intensive use of artificial intelligence, targeting electrical power conversion and electrical energy storage in mobile and stationary applications, covering the entire power range from a few watts up to several gigawatts.

The department is organized in five working groups with a total of about 35 researchers. A highly skilled staff in mechanics, mechatronics, electronics, embedded software, informatics and computational mathematics with long-term experience in industrial R&D projects and technology transfer allows us to successfully support and accompany our customers in addressing today's digitization and tomorrow's digitalization challenges in the energy and power businesses. The close cooperation with the Chair of Power Electronics (LEE) at the University of Erlangen-Nuremberg in Germany provides us with access to the latest fundamental research results and an attractive pool of highly skilled and motivated students.

The group "Data Analytics", headed by Dr. Martin Schellenberger, helps our partners and customers to get the most out of their data in the context of IIoT and Industry 4.0. The group takes an application-oriented approach that includes system analysis, conception, data collection, and finally the development and implementation of intelligent algorithms in industrial processes or in embedded systems.

The group "Energy Technologies", headed by Dr. Richard Öchsner, investigates and optimizes intelligent and decentralized energy systems for the energy and transportation domains. The focus is on the integration of different physical storage systems (i.e., electrical, thermal, hydrogen) and on the intelligent interconnection as well as control – also based on forecasts – of different energy areas (sector coupling, peak load reduction).

The group "Industrial Power Electronics", headed by Markus Billmann, supports our customers in solving power electronic challenges in the field of multi-level converters in all voltage ranges. Whether development support or problem analysis for running facilities and equipment, the list of strengths in the field of troubleshooting of this group is long: longstanding industrial application experience, fast response time, and familiarity with industrial processes.

The "Battery Systems" group, headed by Martin Wenger and Radu Schwarz, is working on innovative solutions for lithium-ion-based electrical energy storage systems for stationary and

1 *DC infrastructure at Fraunhofer IISB.*
© K. Fuchs / Fraunhofer IISB

2 *Dr. Vincent Lorentz, head of the Intelligent Energy Systems department.*
© K. Fuchs / Fraunhofer IISB

INTELLIGENT ENERGY SYSTEMS

Peak Load Reduction – Algorithms and Tools for Peak Shaving Applications in Industrial Environment

mobile applications. The activities range from the development of battery management systems (BMS), algorithms for battery state estimations and predictions, up to the design of full-custom battery systems for large applications like racing cars, submarine exploration robots, airships, and electric gliders.

The group "DC Grids", headed by Bernd Wunder, focuses on innovative solutions for local DC grid systems. Their work ranges from basic research, e.g., on safety and stability issues of DC networks, through concept studies, up to the development of innovative grid components, such as customized DC/DC converters, DC plugs, and protection devices. Bernd Wunder also represents the DC topic on boards such as VDE/DKE, IEC, eMerge Alliance, and IEEE Smart Grid.

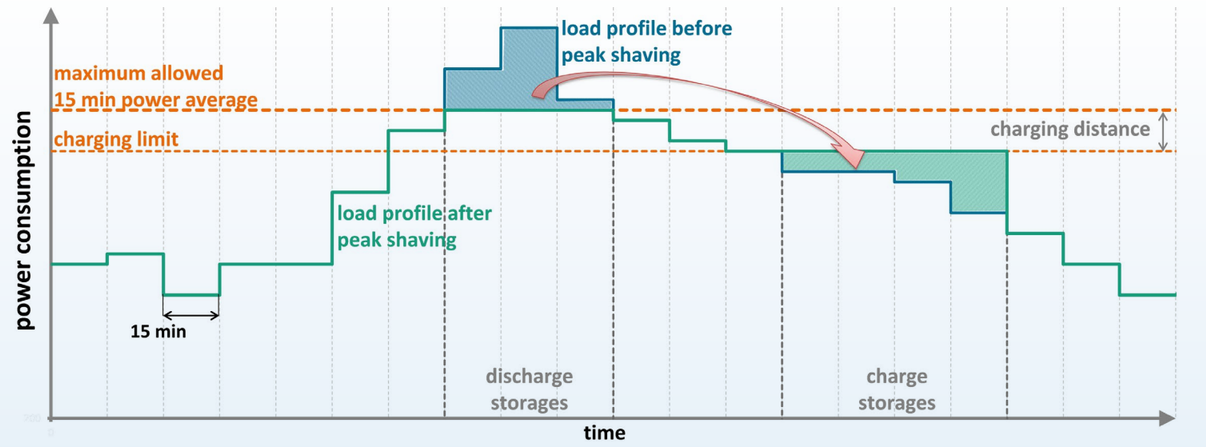
Apart from these highlights, an impressive number of industrial projects were successfully completed. We also had a considerable number of supervised bachelor's and master's theses, scientific publications, and lectures. In addition to our very well received monthly colloquium on power electronics, two seminars were organized for and in cooperation with the Bavarian cluster "Power Electronics".

Sincere thanks to all colleagues in the department for their extraordinary dedication, to all our supporters from industry, politics, and Fraunhofer, and to the entire staff of the IISB.

PEAK LOAD REDUCTION – ALGORITHMS AND TOOLS FOR PEAK SHAVING APPLICATIONS IN INDUSTRIAL ENVIRONMENT

What are power peaks and how can they be shaved?

In industrial environment electricity customer usually pay for the maximum electrical power (EUR per kW, called demand rate) in addition to the electrical energy consumption (EUR per kWh). The maximum power peak within a billing period (e.g. one year) determines the resulting costs. The time series of the electrical power consumption is arithmetically averaged, typically over an interval of 15-minutes. The costs are calculated by multiplying demand rate, which is provided by the energy supplier, by the maximum detected 15-minute consumption peak. Thus, low peak loads enable high saving potentials. Furthermore, investment costs for grid components like transformers can be decreased if lower peak powers are required.



3 *Schematic representation of the algorithm for peak shaving shows important limits.*

Advanced price models allow even higher saving potentials. In Germany, individual grid charges are regulated by a law called Stromnetzentgeltverordnung StromNEV. A part of it is atypical grid usage (Atypische Netznutzung), which restrains the time slots when peak shaving is needed. Another possibility is the intensive grid usage, which requires a usage duration (Benutzungsstundenzahl) of 7000 h and an energy consumption higher than 10 GWh. There are two obvious approaches to reduce the power peaks: Consumers like heat pumps, manufacturing plants etc. could be switched off and generators could be switched on. The problem is that these methods might adversely affect the production and the related infrastructure. Interferences can be avoided if a battery system is used. For the calculation of the dis-/charging power of the electrical energy storage (EES) an algorithm is needed which optimally uses the available battery capacity in order to avoid exceeding a maximum allowed average power.

How do the algorithms work?

At Fraunhofer IISB a set of algorithms was developed around the topic of peak shaving, covering data analysis, dimensioning of battery systems as well as online calculation of dis-/charging power. The development of the algorithms is done in a simulation environment based on MATLAB, which includes a system model of the battery. The model considers losses, degradations and valid operation points with simplified mathematical interrelationships. Model parameters can be transferred from datasheet values or measurements. The input data of the simulation consist of a load profile with a time step of one minute. For example, the yearly load profile measured at the transformer (grid connection point) can be used.

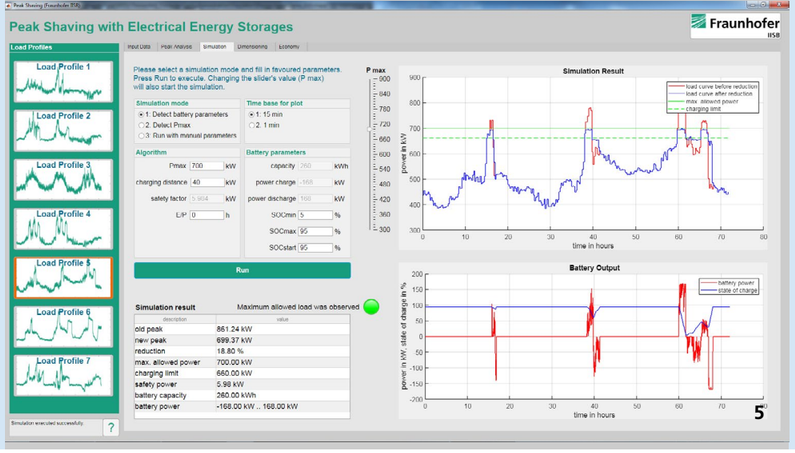
The simulation is used for various tasks: At first, an analysis of the input load profile is done. This includes a statistic evaluation of the appearing peak loads. The next step is the dimensioning of battery and algorithm parameters like capacity and maximum power. Therefore, optimization functions for the detection of the best parameters are used. A part of the dimensioning process is an economic evaluation, which outputs the saving potentials and payback periods. At last, the expected smoothed load profile can be simulated by choosing a parameter set of the dimensioning results (prediction of the resulting time series for peak load reduction). Therefore, the simulation is used to calculate the charging and discharging power of the battery at each time step. The simulations were also used for calculations of the best parameter sets for load profiles of different customers (e.g. energy supply companies and industrial companies).

Once a configuration has been set up, the algorithm continuously calculates the dis-/charging power of the battery: The operator defines a maximum allowed power, which should not be exceeded. The battery system is discharged, if the algorithm detects a predicted 15-minute power above the maximum allowed power. Only the mean value is relevant, which means that power values with a faster time base (e.g. one minute) can be higher than the limit. If there is

INTELLIGENT ENERGY SYSTEMS

Peak Load Reduction – Algorithms and Tools for Peak Shaving Applications in Industrial Environment
Standardization in Modular Multi-Level-Converter Submodules

4



no risk that a peak could happen, the battery system can be charged. To avoid the generation of new peaks because of charging the electrical energy storage, a dead band (charging distance) is introduced. The resulting threshold is called charging limit.

Application at Fraunhofer IISB site

The algorithms are validated by the demonstration platform at the Fraunhofer IISB. The test system consists of a battery system with a capacity of 60 kWh and a maximum power of 100 kW. This configuration was obtained by the dimensioning algorithm of a battery system for the Fraunhofer IISB's power consumption and offers payback periods of approximately three to five years, depending on the price model, if the peak load is reduced by ten percent. The online algorithms are executed by an overall system control, which is an extension of the energy management system. Comparison of measurements and simulation results shows a good accordance. A reduction by 9 % was reached in the test time range.

Extension by thermal energy storages

Battery systems have advantages if fast responses and dynamic transitions are needed. The power and capacity can be extended by use of thermal energy storages. The algorithms also support load shifting with combined heat and power unit (CHP) coupled to thermal energy storages (TES). In this case, the CHP is switched on if high peak loads are expected. A dynamic zone in the TES is reserved for peak shaving operation. This ensures a guaranteed minimum running time of CHP. The battery fills the gap during the startup of the CHP and supports with its high dynamic while peak shaving is active. The CHP's control strategy is represented by a finite state machine, which is easy applicable to existing systems. The battery power is calculated by the same algorithms such as only using the battery system. The algorithms can used by customers as an extension of their energy management system or with a dedicated control system (e.g. PLC).

STANDARDIZATION IN MODULAR MULTI-LEVEL-CONVERTER SUBMODULES

Fraunhofer IISB introduces a new standard for high energy transportation and power quality systems

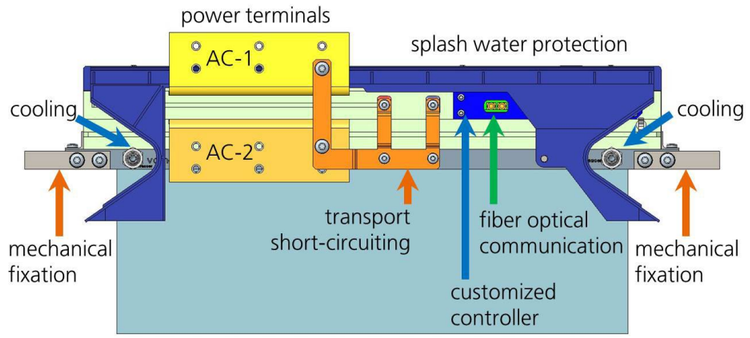
The world's growing demand for electrical energy needs a new concept to ensure a reliable and also flexible power scaling. Today, systems from HVDC to STATCOM are provided by a few big

4 *Employee of Fraunhofer IISB is optimizing parameters of the peak shaving algorithms.*
© K. Fuchs / Fraunhofer IISB

5 *Graphical user interface (GUI) of the simulation environment for peak shaving applications.*

INTELLIGENT ENERGY SYSTEMS

Standardization in Modular Multi-Level-Converter Submodules
Smart Batteries – Innovative Cell Sensors and Artificial Intelligence



Same mechanical family outline – various topologies & voltages

7

players. For scalable high power applications up to the gigawatt-range they all use the principle of modular multi-level converters (MMC). Such systems are based on submodules, mostly voltage source half-, or full-bridge topologies. From up to several tens to thousands of such »megawatt-submodules« are arranged side by side in converter halls, similar to bricks in a wall. The basic functionality is always the same; the design varies in small details depending on the provider.

Comparing existing designs we identified that they all appear very similar, but not good for a future-up-scaling. Enhancing power will lead to more and more »hard-to-handle« mechanical concepts while their aspect ratio will run into an undesirable direction. Spare part exchange time – a major system cost aspect – will increase as a consequence. A similar design pattern within such players is obvious; but all observed modules seem to be »developed for an actual demand«, not considering common future aspects. This means various MMC generations appear quite similar at first glance, but have never been harmonized in terms of interface or rack-mounting compatibility. This leads to a variety in non-compatible mechanical outlines. If we additionally consider reduced product life cycles in high voltage IGBTs, which follow the 600 V to 1700 V IGBT Chip and packaging technology mainstream, this principle will lead to an immense amount of variants. Keep in mind that each version has to provide spare parts for several ten years, which will be a real challenge because downward-compatibility was never a design issue from the start.

At the Fraunhofer IISB, a new approach was developed in cooperation with an independent industrial partner. The IISB has a long term expertise in the field of successful MMC submodule design. Based on a family platform idea, this approach provides identical interfaces and same rack design for various IGBT voltages and topologies. A much better form factor will guarantee not only a volume neutral power enhancement for future generations, but also a nearly ideal mounting space for power electronics components. The design also introduces water cooling for key components as the main capacitor. Our plan is to provide such submodule family members for the global market with centralized perfective maintenance and quality and quality management which will form a downward compatible MMC submodule standard.

SMART BATTERIES – INNOVATIVE CELL SENSORS AND ARTIFICIAL INTELLIGENCE

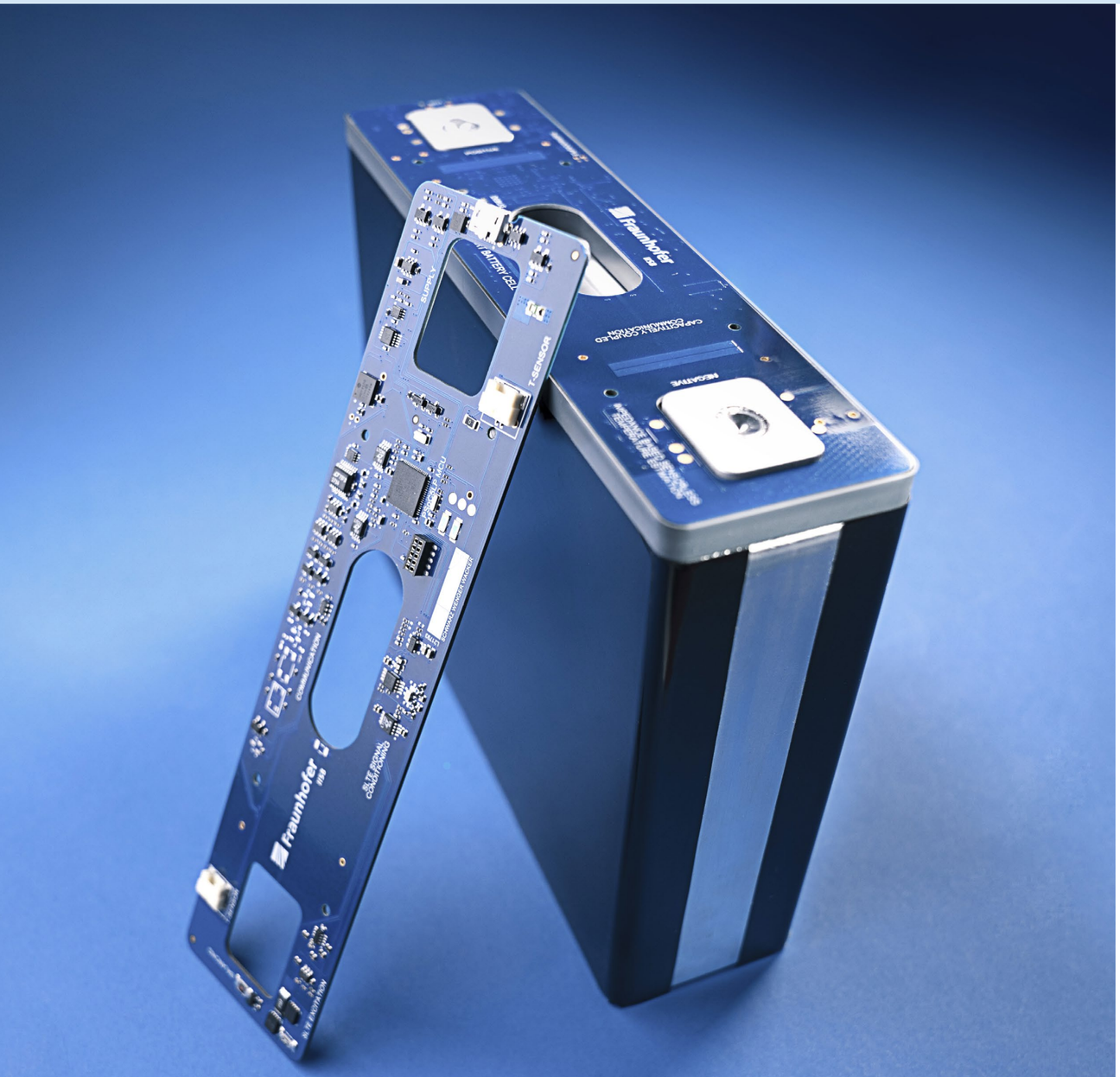
In many applications, the design of battery systems with cells based on Lithium-Ion technology faces challenging boundary conditions, such as weight, temperature range, volume, and cost. In other words, the battery capacity is either too low, or its weight, volume or cost are too high.

6 *Very simple rack mounting and minimized service time.*

7 *Standardized interface, arranged along one side of the submodule, power scaling by Z-, or Y-axis.*

INTELLIGENT ENERGY SYSTEMS

Smart Batteries – Innovative Cell Sensors and Artificial Intelligence
Components and Concepts for DC Microgrids in Industrial and Commercial Applications



8 *Smart battery cell with sensorless temperature estimation and capacitively coupled communication interface.*

Safety margins in the design, introduced to compensate for the inaccuracies of current battery monitoring systems (including their sensors) and battery state estimation, increase this trend.

In order to reduce these design margins and to use the battery systems to its full potential without risking premature ageing or damage, closer monitoring is required. With state-of-the-art monitoring approaches, only cell voltages, scattered temperature information, and the battery current are available at reasonable cost. By integrating innovative sensors, actuators, and intelligence into the battery cell itself, it is possible to create a smart battery cell that is not only able to monitor itself, but also allows gaining a new quality of information that was not accessible with traditional means of battery monitoring.

Following this new design paradigm does not only enable better knowledge of the state of the cell. At the same time, the expected cost savings through reduced design margins in combination with increased freedom in system design have the potential to outweigh the increased cost for a smart cell by far.

Additionally, the information acquired by smart battery cells can help to increase system reliability and availability. Smart battery cells in combination with wireless data transmission, cloud based data storage and methods of machine learning and artificial intelligence pave the way for innovative concepts such as predictive maintenance and fleet management, offering actual added value and enhanced user experience. In the European projects DEMOBASE (this project receives funding from the European Union's Horizon research and innovation programme under grant agreement no. 769900) and AI4DI (this project receives funding from the European Union's Horizon research and innovation programme under grant agreement no. 826060), both funded equally by the German Federal Ministry of Education and Research (BMBF) and the European Commission, these research topics are addressed by the Battery Systems team at Fraunhofer IISB. As part of an ongoing endeavor foxBMS, an open source research platform for battery management systems by Fraunhofer IISB supports and enables these activities.

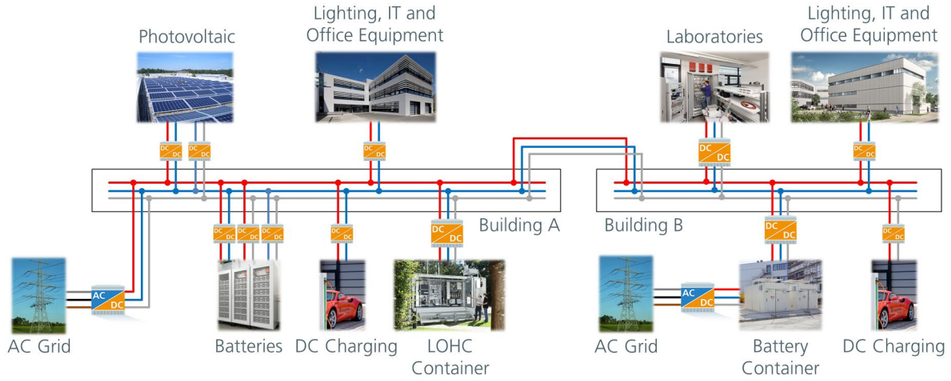
COMPONENTS AND CONCEPTS FOR DC MICROGRIDS IN INDUSTRIAL AND COMMERCIAL APPLICATIONS

With the shift in electrical power system towards a decentralized system with higher share of renewable supply as well as electric mobility, DC based grids will play key roles in the future. This is due to the intrinsic DC characteristic of the main elements, like photovoltaics, electrical energy storage and electric mobility.

INTELLIGENT ENERGY SYSTEMS

Components and Concepts for DC Microgrids in Industrial and Commercial Applications

9 *Arc generated intentionally in a safe test environment at Fraunhofer IISB. The research activities of the DC group at IISB include safety technology for the prevention of electric arcs in DC grids.*



10 *Overview of the DC grid in its current configuration.*

The research area of the "DC Grids" group involves both the challenges as well as the benefits that come with a microgrid based on low voltage direct current. Design of power electronic converters with a focus on efficiency is a part of the group's know-how as well as grid protection and safety elements, stability and grid control, system design and simulation. The group is led by Mr. Bernd Wunder, who is a representative of the IISB on DC topics for various boards like the VDE/DKE or IEC. Due to this high involvement in the normative and standardization process, we support our customers not only with state of the art research, but also with future-proof technologies.

DC Microgrid Installation as Living Lab @ Fraunhofer IISB

A showcase for the application of DC microgrids is the installation at the institute headquarters in Erlangen itself. The installation has already been in service since 2014 and is being continuously expanded. It demonstrates a wide range of devices and concepts that are of interest for industrial or commercial applications. Green energy is sourced from a photovoltaic plant on the roof. Various methods to store excess solar energy are available, ranging from modern lithium-ion battery systems to long-term storage with hydrogen. Power from the microgrid is supplied to office workplaces, laboratories, electric vehicle charging stations, IT equipment, and building lighting. Furthermore, power from the PV or batteries can be fed back into the regular AC installation at the institute to reduce power sourced from the public AC grid at peak load – an important instrument to cut the price of electricity for commercial customers.

This microgrid contains various components that have been developed by Fraunhofer IISB and research partners, such as safety devices, power electronic converters and energy storage systems. The so-called droop control concept uses the grid voltage in order to prioritize the numerous loads and sources, while the safety concept ensures high availability without sacrificing security. As a living lab, the installation is also open for partners from research and industry for the development and testing of new components and concepts.

Contact

Dr.-Ing. Vincent Lorentz
Phone: +49 (0) 9131 761-346
vincent.lorentz@iisb.fraunhofer.de

EVENTS

Young Scientist Dr. Maximilian Rumler receives 3rd Hugo Geiger Prize

1

YOUNG SCIENTIST DR. MAXIMILIAN RUMLER RECEIVES 3RD HUGO GEIGER PRIZE

At the largest internal Fraunhofer networking event, the "Netzwert" symposium, three young scientists were awarded the Hugo Geiger Prize in 2018 for their remarkable doctoral theses. The prize, sponsored by the Bavarian Ministry of Economic Affairs, went to the dissertation of Dr.-Ing. Maximilian Rumler on optical filters for image sensors. The prizes were presented by Franz Josef Pschierer, State Secretary at the Bavarian State Ministry for Economic Affairs and Media, Energy and Technology.

Since 1999, the Fraunhofer-Gesellschaft, together with the Bavarian Ministry of Economic Affairs, has been awarding the Hugo Geiger Prize to outstanding, application-oriented doctoral theses that were prepared in close cooperation with a Fraunhofer Institute. The prize is named after State Secretary Hugo Geiger, patron of the founding meeting of the Fraunhofer-Gesellschaft on March 26th, 1949. Three prizes are awarded, endowed with 5,000, 3,000 and 2,000 euros. The submissions will be judged by a jury of representatives from research and development and industry. The assessment criteria are scientific quality, economic relevance, novelty, and interdisciplinarity of the approaches. This year, the award ceremony took place for the first time as part of the Fraunhofer "Netzwert" symposium.

Dr.-Ing. Maximilian Rumler from Fraunhofer IISB received the third prize for his work on optical filters for image sensors. The principle: Before the incident light hits the pixels of an image sensor – for example in a digital camera – it is separated into the primary colors red, green, and blue by an optical filter. Currently, such filters consist of organic polymers. However, they cannot be reduced in size at will, and they age due to UV radiation and heat. In his dissertation, Rumler dealt with plasmonic filters, which offer an alternative to the color filters commonly used today.

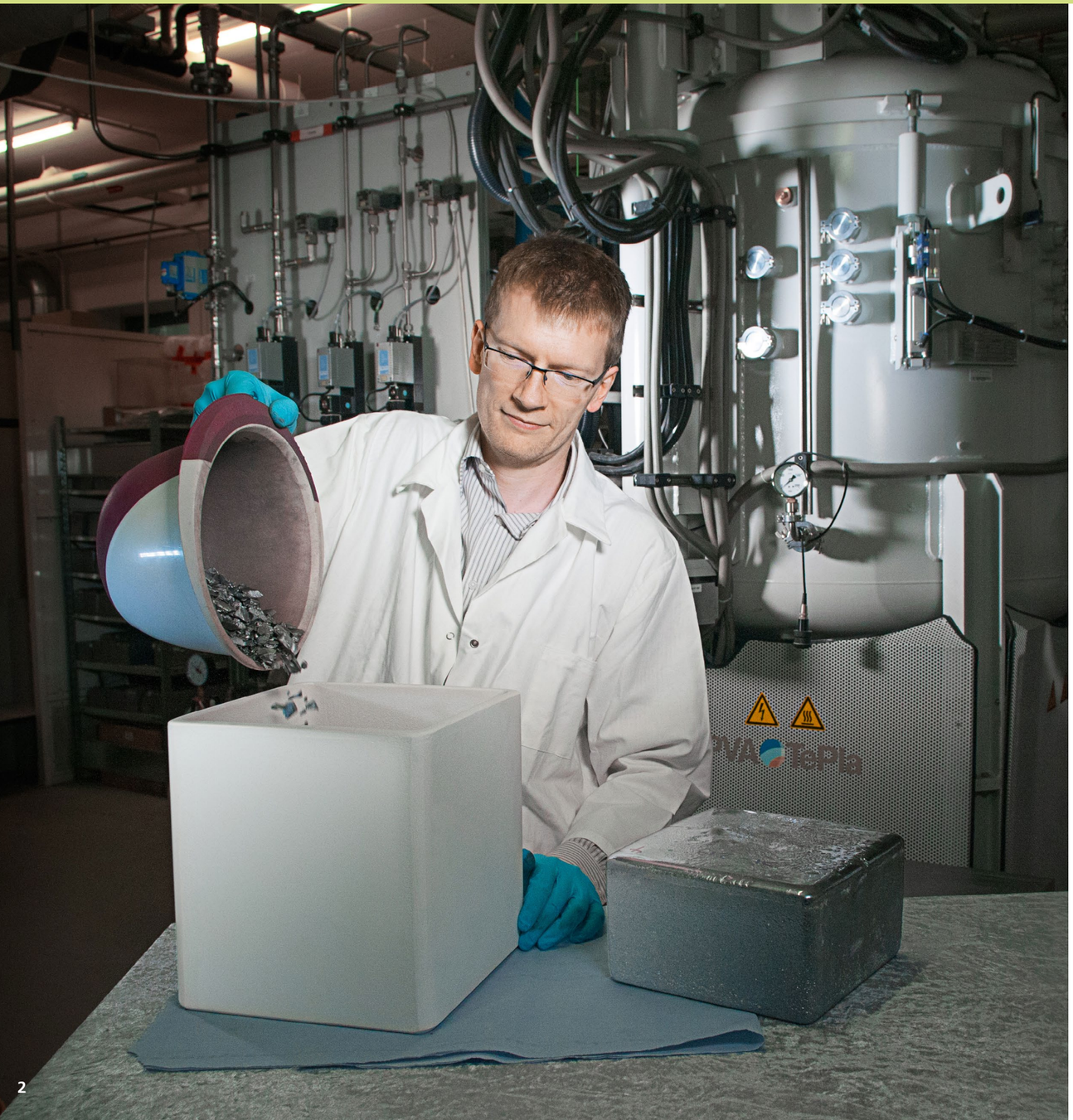
Which plasmonic filter structures are best suited for image sensor technology? Using the "Dr. LiTHO" simulation program from Fraunhofer IISB, he calculated the spectral filter behavior, investigated the influences of various factors, and also reduced the required calculation time. Furthermore, he optimized the embossing process of substrate-compliant imprint lithography and used it for the first time to produce plasmonic filter structures on a large scale. Maximilian Rumler was therefore able to show that large-area photonic structures in the nanometer range can potentially be produced cost-effectively.

1 *Prof. Georg Rosenfeld, Executive Board Member of the Fraunhofer-Gesellschaft for Technology Marketing and Business Models, award winner Dr.-Ing. Maximilian Rumler, former Fraunhofer IISB employee, and Franz Josef Pschierer, State Secretary at the Bavarian State Ministry of Economic Affairs and Media, Energy and Technology, present the 3rd Hugo Geiger Award of the Bavarian State Ministry of Economic Affairs and Media, Energy and Technology.*
© M. Müller / Fraunhofer

EVENTS

Improved Silicon Crystals for Photovoltaics
The Measurement of the Invisible

3



2

IMPROVED SILICON CRYSTALS FOR PHOTOVOLTAICS

Fraunhofer IISB crystal grower receives the Ulrich-Gösele-Young-Scientist-Award 2018

Dr.-Ing. Matthias Trempa from Fraunhofer IISB in Erlangen received the Ulrich-Gösele-Young-Scientist-Award 2018 in honor of the prizewinner's eminent scientific contributions in the field of silicon crystal growth. The knowledge gained in improving the silicon material helps the German supply industry in the field of silicon crystal production to consolidate its position in the photovoltaic market.

The Ulrich-Gösele-Young-Scientist-Award 2018 was presented during the international conference "Crystalline Silicon for Solar Cells" in Sendai, Japan. The prize honors young scientists who have made outstanding scientific and technical contributions in the field of silicon base materials, growing silicon crystals, manufacturing of silicon wafers, or defect engineering specifically for photovoltaic applications. The namesake is Prof. Dr. Ulrich Gösele, who, even after his death, is regarded as one of the world's most renowned scientists in the field of semiconductor physics and technology.

THE MEASUREMENT OF THE INVISIBLE

Innovative measurement method for surface irregularities on semiconductor wafers

Last year's Science Award of the Stiftung Industrieforschung went to Dr.-Ing. Alexander Tobisch for his dissertation "Telecentric Deflectometry for Nanotopography Measurement of Semiconductor Wafers". At Fraunhofer IISB in Erlangen, Dr. Tobisch has developed an innovative optical measurement method that detects the smallest unevenness on reflecting surfaces. The technology enables simple and comprehensive quality control in the semiconductor industry and can help to increase the yield in the manufacturing of microchips.

Alexander Tobisch carried out the development of the theoretical principles as well as the demonstration of the technical feasibility on the basis of two prototypes within the framework of European joint projects with partners from the semiconductor manufacturing and supplier industry. Fraunhofer IISB also cooperates with an established manufacturer who is developing a marketable device.

2 *Dr.-Ing. Matthias Trempa, winner of the Ulrich-Gösele-Young-Scientist-Award, filling a crucible with raw silicon material.*

3 *Jochen Kortmann (left), curator of the Industrial Research Foundation, hands over the first prize of the Industrial Research Foundation 2018 to Dr. Alexander Tobisch (right).*
© J. Hempel / Stiftung Industrieforschung

EVENTS

IISB Research and Development Awards 2018
IISB Microtechnologist Receives Distinction

4

5

The new measuring technology also opens up relatively inexpensive and comparatively simple detection of unevenness in the range of a few nanometers in many areas of application outside semiconductor processing. To emphasize are the high-precision and large-scale measurement of reflective or highly reflective surfaces in the optical industry as well as crack and defect detection during polishing, painting, and coating.

IISB RESEARCH AND DEVELOPMENT AWARDS 2018

The IISB Research and Development Awards were conferred on December 19th, 2018. These awards are given annually by the Institute's Board of Directors in recognition of colleagues who have achieved outstanding results in research and development.

The 2018 award winners were Dr. Christian Kranert for the development of a measurement method to correlate the drawing edge geometry of Cz and Fz silicon crystals with the growth conditions and the team consisting of Stefan Endres, Patrick Meißner, Christoph Seßler, and Moritz Wild for the development of a 22 kW electric vehicle charger demonstrator which redefines the state of the art in terms of efficiency and power density.

IISB MICROTECHNOLOGIST RECEIVES DISTINCTION

Sarah Greger, who completed her apprenticeship as a microtechnologist at the Fraunhofer IISB in 2018, was honoured by the IHK Nuremberg for her examination results and as the best apprentice in the profession of microtechnologist for the 2017/2018 examination year.

At a ceremony on October 23rd, 2018 at the IHK Academy in Nuremberg, IHK President Dirk von Vopelius honoured 63 young merchants and skilled workers who completed their training in the 2018 examination year with excellent results: They completed their apprenticeship in their professions or specialisations as the best and with an overall grade of "very good". A total of 9,600 candidates in Middle Franconia took part in the IHK final examinations in winter 2017/2018 and summer 2018. According to Dirk von Vopelius, the trainees impressively demonstrated their capabilities and commitment. As graduates of the dual training system, they are now highly esteemed employees in industry. He explicitly thanked the dedicated technical colleges as well as the training companies.

4 *From the left: Dr. Jochen Friedrich (Head of the Materials Department), prizewinner Dr. Christian Kranert, Prof. Martin März (director of the IISB)*

5 *From the left: Prof. Martin März (director of the IISB) and the award winners Moritz Wild, Stefan Endres, Christoph Seßler (not in picture: award winner Patrick Meißner)*

EVENTS

Conference Awards for Scientific Research
22nd International Conference on Ion Implantation Technology IIT 2018

7

6

Sarah Greger is now working in the Technology and Manufacturing Department of the IISB and has started her advanced training as a chemical engineer at the same time. Since 1999, the IISB has been educating microtechnologists extremely successfully and in close cooperation with the University of Erlangen-Nuremberg (FAU).

CONFERENCE AWARDS FOR SCIENTIFIC RESEARCH

For the presentation "Impact of Al-Ion Implantation on the Formation of Deep Defects in n-Type 4H-SiC" at the conference IIT 2018 in Würzburg Julietta Weiße (Chair for Electron Devices LEB of the FAU Erlangen-Nuremberg) and her co-authors received the "Best Student Presentation Award". In cooperation with the Fraunhofer IISB and other partners, the work carried out the calculation of compensation in aluminum-implanted n-type SiC, whereby compensation in this case means the capture of free charge carriers in defect centers. In the investigations (including Hall effect and DLTS measurements), compensation levels of over 60 % were determined.

The "Best Poster Award" of the ECSCRM 2018 conference in Birmingham went to the article "Design of a 4H-SiC RESURF n-LDMOS Transistor for High Voltage Integrated Circuits" by Julietta Weiße, Heinz Mitlehner, Lothar Frey and Tobias Erlbacher. Simulation studies were done on a n-LDMOS transistor, in which a compensation structure is integrated by an additional implantation close to the surface, so that a high breakdown voltage (1.3 kV) and a low forward resistance are guaranteed. The design was adapted to a CMOS process developed at IISB. The device is currently being fabricated at LEB and IISB. The lateral device is used, for example, in integrated logic circuits.

Both winning papers were funded as part of the DFG project ER755/1-1.

22ND INTERNATIONAL CONFERENCE ON ION IMPLANTATION TECHNOLOGY IIT 2018

The 22nd International Conference on Ion Implantation Technology IIT 2018 took place from September 16th to 21st, 2018 at the Congress Centrum Würzburg. More than 200 participants from over 20 countries attended the world's most important conference in the field of ion implantation. IIT 2018 was jointly organized by Fraunhofer IISB and Infineon Technologies (Conference

6 *Conference Co-Chair Dr. Reinhard Ploss, CEO of Infineon Technologies AG, at the opening of IIT 2018. © P. Winkelhardt / Fraunhofer IISB*

7 *Sarah Greger with IHK President Dirk von Vopelius (right) and the 2nd Mayor of Nuremberg Christian Vogel at the ceremony on 23 October in the IHK Academy. © K. Fuchs / IHK Nürnberg*

EVENTS

Decentralised Energy Systems for Industry

8 *Prof. Martin März, director of Fraunhofer IISB, welcomes the participants of the annual conference 2018.*
© K. Fuchs / Fraunhofer IISB

Chair: Prof. Lothar Frey, IISB; Conference Co-Chair: Dr. Reinhard Ploss, Infineon; Program Chair: Dr. Volker Häublein, IISB; Chair Local Organizing Committee: Prof. Heiner Ryssel, IISB).

The IIT serves as an open forum for the presentation and discussion of challenges in the field of ion implantation and its solutions.

The topics are:

- Facilities for ion implantation, annealing processes, and measurement technology
- Ion implantation and annealing of semiconductors, but also more and more of other, partly exotic materials
- Ion implantation for devices
- Modeling and Simulation.

The spectrum of participants comprises scientists and engineers from industry and research. With great commitment, the colleagues of the IISB organization team ensured that this year's conference was a success in every respect. The conference was accompanied by a school for ion implantation (September 13th – 15th) and an industrial exhibition.

The scientific conference program consisted of 58 lectures, including 10 invited ones, and 58 posters. The conference proceedings with the scientific publications were published by the IEEE at the beginning of 2019.

DECENTRALIZED ENERGY SYSTEMS FOR INDUSTRY

Fraunhofer IISB Annual Conference 2018

The IISB Annual Conference 2018 focused on "Decentralized Energy Systems for Industry": At the IISB, an industry-oriented test and demonstration platform for intelligent energy supply concepts was developed as a model for distributed energy systems in industry. Examples of innovative components in this overall system are free cooling with a cold storage unit, power-to-chemistry, peak shaving with electrical batteries, DC grids for the efficient interconnection of generators, storages, and consumers as well as DC fast charging as an interface to electromobility.

At the Annual Conference, renowned experts from industry and science presented the current status and research work on decentralized energy systems. During guided tours through the IISB, the participants of the Annual Conference discussed with experts on demonstrators and exhibits.

EVENTS

DRIVE-E 2018

9

DRIVE-E 2018

Five award-winners, 50 students, 100 percent electromobility

Mobility on water, in the air, or on the road, electric drives are no longer a dream of the future. A growing number of young scientists are enthusiastic about this topic. Five of them were awarded the DRIVE-E Study Prize by the Federal Ministry of Education and Research (BMBF) and the Fraunhofer-Gesellschaft at the Deutsches Museum – Verkehrszentrum in Munich on September 12th, 2018, for their impressive theses. The award ceremony is part of an annual summer academy that brings 50 selected students closer to the theory and practice of electromobility in one week with lectures and excursions.

Numerous students from all over Germany applied for the ninth edition of the DRIVE-E Young Investigators Program of the BMBF and Fraunhofer-Gesellschaft. With the Munich University of Applied Sciences as its university partner DRIVE-E stops for the first time in the Bavarian capital. In addition to automotive suppliers such as Robert Bosch GmbH and Schaeffler AG, innovative mobility start-ups from the Munich area were also on site and presented their latest developments. The half-day workshop of the IT service provider NTT Data was dedicated to digitization and autonomous driving. During a guided tour of the BMW plant and BMW-Welt, the students were given a practical insight. The participants also attended presentations by Daimler AG and Audi AG as well as a DriveNow driving event where they were able to put themselves behind the wheel of an electric car. In short: The DRIVE-E Academy convinced again through their unique fusion of theory, practice, and fun.

DRIVE-E was jointly initiated in 2009 by the Federal Ministry of Education and Research (BMBF) and the Fraunhofer-Gesellschaft. With the DRIVE-E Study Award, the BMBF and Fraunhofer-Gesellschaft honor innovative student work on electric mobility. Graduates and students from German universities of applied sciences, universities and other colleges may participate with their scientific theses.

9 *Participants of the DRIVE-E-Academy 2018 in Munich.*
© M. Müller / dedimag / DRIVE-E

EVENTS

Fascination Space

10 *Launch of the TEXUS-55 research rocket on May 31st, 2018 in Esrange near Kiruna in northern Sweden.*
© DLR

FASCINATION SPACE

Erlangen researchers grow crystals in zero-gravity

In order to better understand the formation of defects during the production of crystals, researchers from Fraunhofer IISB and colleagues from the University of Freiburg conducted the "ParSiWal" space experiment. The unmanned research rocket TEXUS 55 of the German Aerospace Center (DLR) served as the carrier vehicle. TEXUS 55 was launched on May 31st, 2018 from the Esrange space centre near Kiruna in northern Sweden. This experiment in zero-gravity is aimed at optimizing the production of silicon crystals for photovoltaic applications on Earth. ParSiWal ("Determination of the critical velocity for particle engulfment during the directional solidification of solar silicon in space") is used specifically to investigate the undesired incorporation of silicon carbide and silicon nitride particles that can occur during the solidification of silicon crystals from a silicon melt. The incorporation of such particles reduces the yield and later quality of solar cells.

The ParSiWal project is part of DLR's "Research under Space Conditions" programme and is supported by DLR Space Management with funds from the Federal Ministry of Economics and Technology (BMWi).

ParSiWal continues the long tradition of Erlangen space experiments in the field of crystal growth. Researchers from Erlangen have already grown technical crystals on earlier rocket flights (1984, 1988, 1989, 1992, 2015, 2016) and even on the Space Shuttle (1983, 1985, 1993). In addition, the CrysMAS® software developed at Fraunhofer IISB passed an elaborate qualification procedure at the European Space Agency ESA about 15 years ago.

Since then, the CrysMAS® program, which calculates temperature distributions in furnaces, has been used by researchers to simulate material science experiments on the International Space Station ISS.

EVENTS

Cutting-Edge FIB System at the IISB

12

11

CUTTING-EDGE FIB SYSTEM AT THE IISB

On June 20th, 2018, researchers at the IISB celebrated the commissioning of a high-rate plasma focused ion beam system (FIB) as part of the Microelectronics Research Factory Germany (FMD). Through the networking in the FMD, a cooperation network of eleven Fraunhofer and two Leibniz institutes funded by the BMBF, the unique research infrastructure in Erlangen will also be made accessible to customers and cooperation partners across disciplinary and institute boundaries.

The system supplied by FEI/Thermo Fisher AG is a xenon plasma focused ion beam system with an ion beam current of up to 2.5 µA, which is combined with a scanning electron microscope (SEM) with a resolution of a few nanometers. In addition to instruments of the latest EDX and EBSD generation from Oxford Instruments for the analysis of material compositions and crystal orientations, for example, a micro tensile module from Kammrath & Weiss GmbH can also be integrated into the system. This allows to load samples with forces of up to 5000 N at temperatures of up to 500 °C and to analyze changes in geometry, topography and morphology with software support. In particular, the combination with an ultra-short pulse laser – a strategic investment of the institute – and established lock-in thermography allows researchers to gain in-depth insights into the interactions and failure mechanisms of materials, devices, and systems.

11 *In-situ analysis of material composition and crystal orientation in new high-rate plasma FIB system at Fraunhofer IISB.*
© K. Fuchs / Fraunhofer IISB

12 *Inauguration of the new high-rate plasma FIB system at Fraunhofer IISB, which was installed within the framework of the Forschungsfabrik Mikroelektronik Deutschland (FMD).*
© K. Fuchs / Fraunhofer IISB

NAMES AND DATA

GUEST SCIENTISTS

Choi, H.-H.
August 30 - 31, 2018
South Korea
National Institute for Nanomaterials Technology (NINT) / Postech
Diskussion über Projekt (GRDC) bzgl. der technischen Themen und Organisation

Gu, Z.
September 1, 2018 - August 30, 2019
China
Shanghai Institute of Microsystem and Information Technologx, CAS, Shanghai
Design and Fabrication of SiC Power Transistors, Process development, structue design, gate dielectric engineering

Jiho, S.
August 26 - 29, 2018
South Korea
Kwangwoon University

Kang, M.-J.
August 27 - 31, 2018
South Korea
National Institute for Nanomaterials Technology (NINT) / Postech
Diskussion über Projekt (GRDC) bzgl. der technischen Themen und Organisation

Kim, H.-K.
August 27 - 31, 2018
South Korea
National Institute for Nanomaterials Technology (NINT) / Postech
Diskussion über Projekt (GRDC) bzgl. der technischen Themen und Organisation

Kim, S.
August 27 - 31, 2018
South Korea
National Institute for Nanomaterials Technology (NINT) / Postech
Diskussion über Projekt (GRDC) bzgl. der technischen Themen und Organisation

Lee, N.-S.
August 30 - 31, 2018
South Korea
National Institute for Nanomaterials Technology (NINT) / Postech
Diskussion über Projekt (GRDC) bzgl. der technischen Themen und Organisation

Li, M.
July 30, 2018 - August 3, 2018
China
Beijing Century Goldray
Projektbesprechung bezüglich Bauelementeentwicklung und Herstellung, sowie Prozessoutsourcing

Michalowski, P.
September 25 - 27, 2018
Poland
Institute of Electronic Materials Technology
Fundamental principles and applications of Secondary Ion Mass Spectromtery

Ni, W.
July 30, 2018 - August, 3, 2018
China
Beijing Century Goldray
Projektbesprechung bezüglich Bauelementeentwicklung und Herstellung, sowie Prozessoutsourcing

Papagiannopoulos, A.
July 9, 2018 - August 31, 2018
France
INP Grenoble
Setup of a Hardware in the Loop Test bench for a Battery Management

Sang-Mo, K.
August 26 - 29, 2018
South Korea
Kwangwoon University

Seong-Ji, M.
August 26 - 29, 2018
South Korea
Kwangwoon University

Shin, H.-K.
August 30 - 31, 2018
South Korea
National Institute for Nanomaterials Technology (NINT) / Postech
Diskussion über Projekt (GRDC) bzgl. der technischen Themen und Organisation

Yeong-Jae, L.
August 26 - 29, 2018
South Korea
Kwangwoon University

Xu, M.
July 30, 2018 - August 3, 2018
China
Beijing Century Goldray
Projektbesprechung bezüglich Bauelementeentwicklung und Herstellung, sowie Prozessoutsourcing

NAMES AND DATA

PATENTS (GRANTED IN 2018)

Bauer, A.; Erlbacher, T.; Schwarzmann, H.:
Integrierter Kondensator und Verfahren zum Herstellen desselben
DE 10 2014 200 869 A1

Bauer, A.; Erlbacher, T.; Schwarzmann, H.:
Integrated capcaitor and method for producing the same
US 2016/0365408 A1

Berberich, S.; Schwarzmann, H.:
Vorrichtung und Verfahren zur Ladungsträgergenerierung
DE 10 2008 023 517.2

Dadzis, K.; Dietrich, M.; Freudenberg, B.; Friedrich, J.; Gruendig-Wendrock, B.; Gruetzner, S.; Krause, A.; Nauert, D.; Reimann, C.; Trempa, M.:
Vorrichtung und Verfahren zur Herstellen von Silizium-Blöcken
10 2011 082 628.9

Endres, S.; Zeltner, S.:
Leistungselektronische Schaltung und System mit derselben

Erlbacher, T.:
Verfahren, Halbleiterdetektor und Detektoranordnung zur Detektion von Sonnenlicht
EP 15 197 783.2

Erlbacher, T.:
Verfahren und Detektoranordnung zur Detektion von Sonnenlicht
US 2016/0172524 A1

Erlbacher, T.; Huerner, A.:
Monolithically integrated semiconductor switch particularly circuit breaker
US20170323884A1

Erlbacher, T.; Huerner, A.:
Schottky diode and method for its manufacturing
US 2018-0108788 A1

Friedrich, J.; Hussy, S.:
Verfahren zur Reduzierung von Makrodefekten bei der Herstellung von Einkristallen oder einkristallinen Schichten
11 2007 003 634.6-43

Friedrich, J.; Reimann, C.; Schneider, V.:
Verfahren zur Aufreinigung eines Tiegels
DE 102012201116.1

Hopperdietzel, R.:
Device for switching a semiconductor-based switch and sensor for detecting a current change velocity at a semiconductor based switch
US 2017/0104338 A1

Lazareva, I.; Nutsch, A.:
Verfahren zur Bestimmung der Topografie einer Oberfläche eines Objekts
DE 10 2010 019 668.1

Lewke, D.; Schellenberger, M.; Tobisch, A.:
Verfahren zur Überprüfung eines Trennschrittes bei der Zerteilung eines flachen Werkstückes in Teilstücke
DE 10 2015 225 929 A1

Wahle, M.; Dorn, J.; Gambach, H.; Billmann, M.:
Submodul mit Kurzschlussstromentlastung
EP2748906 A1

NAMES AND DATA

CONFERENCES, WORKSHOPS, FAIRS, AND EXHIBITIONS

12. Anwenderkongress Steckverbinder
Würzburg, Germany, April 4, 2018

15. Vibrometer Anwenderkonferenz
Waldbronn, Germany, November 13, 2018

16th Lithography Simulation Workshop of the IISB
Gräfenberg, Germany, September 13 - 15, 2018

17. Nutzergruppentreffen der GMM-VDE/VDI-Fachgruppe 1.2.6 "Prozesskontrolle, Inspektion und Analytik"
Fraunhofer IISB, Erlangen, Germany, March 15, 2018

21. Workshop der GMM-VDE/VDI-Fachgruppe 1.2.3 "Abscheide- und Ätzverfahren"
Fraunhofer IISB, Erlangen, Germany, December 5, 2018

35th EU PVSEC 2018, European Photovoltaic Solar Energy Conference and Exhibition
Brussels, Belgium, September 24 - 28, 2018

43. Nutzergruppentreffen der GMM-VDE/VDI-Fachgruppe 1.2.4 "Heißprozesse und RTP"
Fraunhofer IISB, Erlangen, Germany, April 11, 2018

59. Nutzergruppentreffen der GMM-VDE/VDI-Fachgruppe 1.2.2 "Ionenimplantation"
Fraunhofer IISB, Erlangen, Germany, April 12, 2018

64th IEEE Holm Conference on Electrical Contacts
Albuquerque, USA, October 14 - 18, 2018

233rd ECS Meeting, Spring Meeting of the Electrochemical Society
Seattle, USA, May 13 - 17, 2018

CEFC 2018, 18th IEEE Conference on Electromagnetic Field Computation
Hangzhou, China, October 28 - 31, 2018

CIPS 2018, 10th International Conference on Integrated Power Electronics Systems
Stuttgart, Germany, March 20 - 22, 2018

CSSC-10, 10th International Workshop on Crystalline Silicon for Solar Cells
Sendai, Japan, April 8 - 11, 2018

DCIS 2018, Conference on Design of Circuits and Integrated Systems
Lyon, France, November 14 - 16, 2018

DGKK Arbeitskreis "Massive Halbleiterkristalle"
Erlangen, Germany, October 10, 2018

ECCG6, 6th European Conference on Crystal Growth
Varna, Bulgaria, September 16 - 20, 2018

ECPE Workshop "The Future of Simulation in PE Packaging for Thermal and Stress Management"
Nuremberg, Germany, November 20 - 21, 2018

ECSCRM 2018, 12th European Conference on Silicon Carbide and Related Materials
Birmingham, UK, September 2 - 6, 2018

EFECS 2018, European Forum for Electronic Components and Systems
Lisbon, Portugal, November 20 - 22, 2018

EMLC 2018, 34th European Mask and Lithography Conference
Grenoble, France, June 18 - 20, 2018

E-Motive, 10. Expertenforum Elektrische Fahrzeugantriebe
Stuttgart, Germany, September 13, 2018

EMRS Fall Meeting 2018
Warsaw, Poland, September 17 - 20, 2018

EOSAM 2018, European Optical Society Biennial Meeting
Delft, Netherlands, October 8 - 12, 2018

ESREF 2018, 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis
Aalborg, Denmark, October 1 - 5, 2018

ESTC 2018, IEEE 7th Electronics System-Integration Technology Conference
Dresden, Germany, September 18 - 21, 2018

EuMC 2018, 48th European Microwave Conference
Madrid, Spain, September 25 - 27, 2018

EuroSimE 2018, 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems
Toulouse, France, April 15 - 18, 2018

GACCG / DKT2018, 1st German-Austrian Conference on Crystal Growth
Vienna, Austria, February 14 - 16, 2018

GMM Workshop "New Developments in Deposition / Etching"
Erlangen, Germany, December 5, 2018

IEEE IESES 2018, 1st International Conference on Industrial Electronics for Sustainable Energy Systems
Hamilton, New Zealand, January 31 - February 2, 2018

IEEE-PEMC, 18th International Conference on Power Electronics and Motion Control
Budapest, Hungary, August 26 - 30, 2018

International Conference on Ion Implantation Technology 2018 School
Würzburg, Germany, September 13 - 15, 2018

IIT 2018, 22nd International Conference on Ion Implantation Technology
Würzburg, Germany, September 16 - 21, 2018

INTELEC 2018, International Telecommunications Energy Conference
Torino, Italy, October 7 - 11, 2018

International Workshop E-Mobility & Circular Economy
Freiberg, Germany, June 6 - 7, 2018

IPEC 2018, ECCE Asia, International Power Electronics Conference
Niigata, Japan, May 20 - 24, 2018

ITEC 2018, IEEE Transportation Electrification Conference
Long Beach, USA, June 13 - 15, 2018

IWMCG-9, 9th International Workshop on Modeling in Crystal Growth
Big Island, Hawaii, October, 21 - 24, 2018

IWN 2018, 10th International Workshop on Nitride Semiconductors
Kanazawa, Japan, November 11 - 16, 2018

Karrieremesse ORTE
Freiberg, Germany, January 11, 2018

Kooperationsforum Interieur im Automobil, Bayern Innovativ
Kongresshalle, Bamberg, Germany, March 14, 2018

Nutzergruppentreffen der GMM-VDE/VDI-Fachgruppe 1.2.3 "Abscheide- und Ätzverfahren"
Fraunhofer IISB, Erlangen, December 4, 2018

NAMES AND DATA

CONTINUATION: CONFERENCES, WORKSHOPS, FAIRS, AND EXHIBITIONS

Nutzertreffen der GMM-Fachgruppe 1.2.6
„Prozesskontrolle, Inspektion & Analytik“
Erlangen, Germany, March 15, 2017

ODF 2018, 11th International Conference on Optics-photonics Design & Fabrication
Hiroshima, Japan, November 28 - 30, 2018

PCIM Europe 2018, International Exhibition and Conference for Power Electronic, Intelligent Motion, Renewable Energy and Energy Management
Nuremberg, Germany, June 5 - 7, 2018

Printed Electronics Europe
Berlin, Germany, April 10 - 12, 2018

P-Seminar “Kristallzüchtung” der Bertolt-Brecht Schule
Nuremberg, Germany, 2018

P-Seminar Schulwettbewerb „Wer züchtet den schönsten Kristall?“ des Gymnasiums Eckental
Nuremberg, Germany, 2018

Semicon Europa 2018, Strategic Materials Conference
Munich, Germany, November 11 - 13, 2018

Semicon West 2018, Internationale Fachmesse für Halbleiterprodukte
San Francisco, USA, July 9 - 12, 2018
SISPAD 2018, Conference on Simulation of Semiconductor Processes and Devices
Austin, United States, September 24 - 26, 2018

SNEC, 12th International Photovoltaic Power Generation and Smart Energy Conference & Exhibition 2018
Shanghai, China, May 28 - 30, 2018

SPIE Advanced Lithography 2018
San Jose, February 25 - March 1, 2018

SPIE Optical Systems Design
Frankfurt, Germany, May 14 - 17, 2018

SPIE Photomask Technology + EUV Lithography 2018
Monterey, USA, September 17 - 20, 2018

SSDM 2018, 50th International Conference on Solid State Devices and Materials
Tokyo, Japan, September 9 - 13, 2018

SUPERAID7 Workshop “Process Variations from Equipment Effects to Circuit and Design Impacts”
Dresden, Germany, September 3, 2018

Technologieseminar DC-Smart Grid – Netz- und Energiemanagement in der Produktion
Stuttgart, Germany, June 7, 2018

WiPDA 2018, IEEE 6th Workshop on Wide Bandgap Power Devices and Applications
Atlanta, USA, October 31 - November 2, 2018

WODIM 2018, 20th Workshop on Dielectrics in Microelectronics
Berlin, Germany, June 10 - 14, 2018

PUBLICATIONS

Bach, H. L.; Endres, T.; Dirksen, D.; Zischler, S.; Bayer, C. F.; Schletz, A.; Maerz, M.:
Ceramic Embedding as Packaging Solution for Future Power Electronic Applications
Int. Power Electronics Conference (ECCE IPEC) 2018, Niigata
DOI: 10.23919/IPEC.2018.8507647

Bach, H. L.; Yu, Z.; Letz, S.; Bayer, C. F.; Waltrich, U.; Schletz, A.; Maerz, M.:
Vias in DBC Substrates for Embedded Power Modules
10th Int. Conference on Integrated Power Electronics Systems (CIPS) 2018, pp. 144-148
ISBN: 978-3-8007-4540-1

Baehr, T.; Ghosh, M.; Kranert, C.; Reimann, C.; Morche, C.:
Development of methods for reducing the red zone in the top region of mc-silicon ingots
Proceedings of 35th European Photovoltaic Solar Energy Conference and Exhibition (2018), pp. 488-492
DOI: 10.4229/35thEUPVSEC20182018-2AV.1.11

Baer, E.; Lorenz, J.:
The effect of etching and deposition processes on the width of spacers created during self-aligned double patterning
Proceedings of International Conference on Simulation of Semiconductor Processes and Devices, SISPAD 2018, pp. 236-239
DOI: 10.1109/SISPAD.2018.8551649

Banzhaf, S.; Kenntner, J.; Grieb, M.; Schwaiger, S.; Erlbacher, T.; Bauer, A. J.; Frey, L.:
Stress Reduction in High Voltage MIS Capacitor Fabrication
19th International Symposium Power Electronics Ee2017, October 19-21 (2017) Novi Sad, Serbia
DOI: 10.1109/PEE.2017.8171664

Bauer, A.; Baer, E.; Erlbacher, T.; Friedrich, J.; Lorenz, J.; Rommel, M.; Schellenberger, M.:
Elektronik
Angewandte Nanotechnologie, K.-H. Haas, G. Tovar (Ed.), Fraunhofer Verlag, Stuttgart, 2018, pp. 98-115
ISBN: 978-3839609187

Bayer, C. F.; Diepgen, A.; Filippi, T.; Fuchs, C.; Wuestefeld, S.; Kellner, S.; Waltrich, U.; Schletz, A.:
Electrochemical Corrosion on Ceramic Substrates for Power Electronics - Causes, Phenomenological Description, and Outlook
10th Int. Conference on Integrated Power Electronics Systems (CIPS) 2018, pp. 161-167
ISBN: 978-3-8007-4540-1

NAMES AND DATA

CONTINUATION: PUBLICATIONS

Bayer, C. F.; Frey, L.:
Untersuchung der elektrischen Feldstärke und des Teilentladungsverhaltens an keramischen Schaltungsträgern
Dissertation, Friedrich-Alexander-Universität Erlangen Nürnberg, 2018

Belete, Z.; Baer, E.; Erdmann, A.:
Modeling of block copolymer dry etching for directed self-assembly lithography
Proceedings of SPIE Advanced Lithography 2018, paper 105890U, 12 pages
DOI: 10.1117/12.2299977

Bilbao-Guillerna, A.; Eachambadi, R.T.; Cadot, G.B.J.; Axinte, D.A.; Billingham, J.; Stumpf, F.; Beuer, S.; Rommel, M.:
Novel Approach Based on Continuous Trench Modelling to Predict Focused Ion Beam Prepared Freeform Surfaces
Journal of Materials Processing Technology 252 (2018), pp. 636-642
http://doi.org/10.1016/j.jmatprotec.2017.10.024

Cerezuela Barreto, M.; Roeder, G.; Steinhoff, M.; Schellenberger, M.; and Bauer, A. J.:
Advances in thermal laser separation: process monitoring in a kerf-free laser-based cutting technology to ensure high yield
Procedia CIRP, vol. 74, pp. 645-648, 01.01.2018
https://doi.org/10.1016/j.procir.2018.08.056

Chen, S.; Jiang, L.; Buckwell, M.; Jing, X.; Ji, Y.; Grustan-Gutierrez, E.; Hui, F.; Shi, Y.; Rommel, M.; Paskaleva, A.; Benstetter, G.; Ng, W.H.; Mehonic, A.; Kenyon, A.J.; Lanza, M.:
On the Limits of Scalpel AFM for the 3D Electrical Characterization of Nanomaterials
Advanced Functional Materials 2018 (2018) 1802266
https://doi.org/10.1002/adfm.201802266

Dejkameh, A.; Erdmann, A.; Evanschitzky, P.:
Fourier ptychography for lithography high NA systems
Proceedings of SPIE Advanced Lithography 2018, paper 106940B
DOI: 10.1117/12.2311332

Derluyn, J.; Germain, M.; Meissner, E.:
Taking the next step in GaN: Bulk GaN substrates and GaN-on-Si epitaxy for electronics
Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion (Eds. G. Meneghesso, M. Meneghini, Matteo, E. Zanoni) Springer (2018), pp. 1-28
ISBN: 978-3-319-77993-5

Dresel, F.; Tham, N.; Erlbacher, T.; Schletz, A.:
Lifetime Testing Method for Ceramic Capacitors for Power Electronics Applications
10th Int. Conference on Integrated Power Electronics Systems (CIPS) 2018
ISBN: 978-3-8007-4540-1

Dresel, F.; Letz, S.; Zischler, S.; Schletz, A.; Novak, M.:
Selective silver sintering of semiconductor dies on PCB
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018, Nuremberg
ISBN: 978-3-8007-4646-0

Eckardt, B.; Wild, M.; Joffe, C.; Zeltner, S.; Endres, S.; Maerz, M.:
Advanced Vehicle Charging Solutions Using SiC and GaN Power Devices
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018, Nuremberg
ISBN: 978-3-8007-4646-0

Endruschat, A.; Novak, C.; Gerstner, H.; Heckel, T.; Joffe, C.; Maerz, M.:
A Universal SPICE Field-Effect Transistor Model Applied on SiC and GaN Power Transistors
IEEE Transactions on Power Electronics, Dec. 2018
DOI: 10.1109/TPEL.2018.2889513

Erdmann, A.; Evanschitzky, P.; Mezilhy, H.; Philipsen, V.; Hendrickx, E.; Bauer, M.:
Attenuated PSM for EUV: Can they mitigate 3D mask effects?
Proceedings of SPIE Advanced Lithography 2018, paper 1058312
DOI: 10.1117/12.2299648

Erlbacher, T.; Huerner, A.; Zhu, Y.; Bach, L.; Schletz, A.; Zuerbig, V.; Pinti, L.; Kirste, L.; Giese, C.; Nebel, C. E.; Bauer, A. J.; Frey, L.:
Electrical properties of Schottky-Diodes based on B Doped Diamond
Material Science Forum 924 (2018), pp. 164-167
DOI: 10.4028/www.scientific.net/MSF.924.931

Erlekampf, J.; Kaminzky, D.; Rosshirt, K.; Kallinger, B.; Rommel, M.; Berwian, P.; Friedrich, J.; Frey, L.:
Influence and mutual interaction of process parameters on the Z1/2 defect concentration during epitaxy of 4H-SiC
Materials Science Forum Vol 924 (2018), pp. 112-115
DOI: 10.4028/www.scientific.net/MSF.924.112

NAMES AND DATA

CONTINUATION: PUBLICATIONS

Förthner, M.; Girschikofsky, M.; Rumler, M.; Stumpf, F.; Rommel, M.; Hellmann, R.; Frey, L.:
One-step nanoimprinted Bragg grating sensor based on hybrid polymers
Sensors and Actuators A-Physical, 283, pp. 298-304
DOI: 10.1016/j.sna.2018.09.053

Gerstner, H.; Endruschat, A.; Heckel, T.; Joffe, C.; Eckardt, B.; Maerz, M.:
Non-linear Input Capacitance Determination of WBG Power FETs using Gate Charge Measurements
IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2018, pp. 247-253
DOI: 10.1109/WiPDA.2018.8569089

Girschikofsky, M. G.; Rosenberger, M.; Förthner, M.; Rommel, M.; Frey, L.; Hellmann, R.:
Flexible thin film bending sensor based on Bragg gratings in hybrid polymers
Proceedings of the Optical Sensing and Detection V 2018
DOI: 10.1117/12.2303820

Gosses, K.; Kaiser, J.; Ott, L.; Schulz, M.; Fersterra, F.; Wunder, B.; Han, Y.; Lavery, M.; Maerz, M.:
Fault Considerations of Non-Isolated Electric Vehicle Chargers with a Mutual DC Supply
IEEE Transportation Electrification Conference (ITEC) 2018, Long Beach, CA
DOI: 10.1109/ITEC.2018.8450243

He, R.; Heyn, W.; Thiel, F.; Pérez, N.; Damm, C.; Pohl, D.; Rellinghaus, B.; Reimann, C.; Beier, M.; Friedrich, J.; Zhu, H.; Ren, Z.; Nielsch, K.; Schierning, G.:
Thermoelectric properties of silicon and recycled silicon sawing waste
Journal of Materiomics (2018)
DOI: https://doi.org/10.1016/j.jmat.2018.11.004.

He, Z.; Xu, Z.; Rommel, M.; Yao, B.; Liu, T.; Song, Y.; Fang, F.:
Investigation of Ga ion implantation-induced damage in single-crystal 6H-SiC
Journal of Micromanufacturing I-9 (2018), pp. 1-9
https://doi.org/10.1177/2516598418785507

Heckel, T.:
Charakterisierung dynamischer Eigenschaften und Modellbildung neuartiger Leistungshalbleiterbauelemente auf Basis von SiC und GaN
Verlag Dr. Hut, München, 2018
ISBN: 978-3-8439-3764-1

Heckel, T.; Zeltner, S.; Eckardt, B.; Maerz, M.;
Fast Switching with GaN and Dynamic On-Resistance from Application View-Point
2018 GaN Power Electronics Roadmap, Journal of Physics D: Applied Physics 51(16), 2018
https://doi.org/10.1088/1361-6463/aaaf9d

Huerner, A.; Heckel, T.; Enduschat, A.; Erlbacher, T.; Frey, L.:
Analytical Model for the Influence of the Gate-Voltage on the Forward Conduction Properties of the Body-Diode in SiC-MOSFETs
Material Science Forum 924 (2018), pp. 901-904
DOI: 10.4028/www.scientific.net/MSF.924.901

Hutzler, A.; Matthus, C.; Rommel, M.; Jank, M.; Frey, L.:
Large-Area Layer Counting of 2D Materials via Visible Reflection Spectroscopy
Proceedings of the 19th International Microscopy Congress (IMC19), Sydney 2018

Hutzler, A.; Schmutzler, T.; Jank, M.P.M.; Branscheid, R.; Unruh, T.; Spiecker, E.; Frey, L.:
Unravelling the Mechanisms of Gold–Silver Core–Shell Nanostructure Formation by in Situ TEM Using an Advanced Liquid Cell Design
Nano Letters, Bd. 18, H. 11
DOI: 10.1021/acs.nanolett.8b03388

Ismail, M.; Evanschitzky, P.; Erdmann, A.; Bottiglieri, G.; van Setten, E.; Fliervoet, T.:
Simulation study of illumination effects in high-NA EUV lithography
Proceedings of SPIE Advanced Lithography 2018, paper 106940H
DOI: 10.1117/12.2315091

Kaiser, J.; Schork, F.; Gosses, K.; Han, Y.; Schulz, M.; Ott, L.; Wunder, B.; Maerz, M.:
Converter Overvoltage Protection for DC-Grids
IEEE 40th Int. Telecommunications Energy Conference (INTELEC), 2018
DOI: 10.1109/INTLEC.2018.8612423

Kallinger, B.; Kaminzky, D.; Berwian, P.; Friedrich, J.; Oppel, S.:
Optical stressing of 4H-SiC material and devices
Materials Science Forum Vol 924 (2018), pp. 196-199
DOI: https://doi.org/10.4028/www.scientific.net/MSF.924.196

Kocher, M.; Rommel, M.; Erlbacher, T.; Bauer, A. J.:
Influence of Al Doping Concentration and Annealing Properties on TiAl Based Ohmic Contacts on 4H-SiC
Material Science Forum 924 (2018), pp. 393-396
DOI: 10.4028/www.scientific.net/MSF.924.393

NAMES AND DATA

CONTINUATION: PUBLICATIONS

Kreutzer, O.; Billmann, M.; Gerner, M.; Maerz, M.:
A 3.6 kV full SiC fuel cell boost converter for high power electric aircraft
IEEE Transportation Electrification Conference (ITEC) 2018, Long Beach, CA
DOI: 10.1109/ITEC.2018.8450229

Kreutzer, O.; Billmann, M.; Maerz, M.:
Is an antiparallel SiC-Schottky diode necessary - Calorimetric Analysis of SiC-MOSFETs switching behavior
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018, Nuremberg
ISBN 978-3-8007-4646-0

Letz, S.; Farooghian, A.; Simon, F. B.; Schletz, A.:
Modeling the rate-dependent inelastic deformation of porous polycrystalline silver films
Microelectronics reliability 88-90 (2018), pp.1113-1117
DOI: 10.1016/j.microrel.2018.07.084

Lorentz, V. R. H.; Waller, R.; Waldhoer, S.; Wenger, M.; Gepp, M.; Schwarz, R.; Koffel, S.; Wacker, S.; Akdere, M.; Giegerich, M.; Maerz, M.:
Power Antifuse Device to Bypass or Turn-off Battery Cells in Safety-Critical and Fail-Operational Systems
IEEE Int. Conference on Industrial Electronics for Sustainable Energy Systems (IESES 2018), Hamilton, New Zealand
DOI: 10.1109/IESES.2018.8349850

Lorenz, J.; Asenov, A.; Baer, E.; Barraud, S.; Kluepfel, F.; Millar, C.; Nedjalkov, M.:
Process variability for devices at and beyond the 7 nm node
ECS Journal of Solid State Science and Technology 11 (2018), pp. 595-601
DOI: 10.1149/2.0051811jss

Lorenz, J.; Asenov, A.; Baer, E.; Barraud, S.; Millar, C.; Nedjalkov, M.:
Process variability for devices at and beyond the 7 nm node
Proceedings of the 233rd Meeting of the Electrochemical Society (2018), pp. 113-124
DOI: 10.1149/08508.0113ecst

Lorenz, L.; Erlbacher, T.; Hilt, O.:
Future technology trends
Wide Bandgap Power Semiconductor Packaging, Woodhead Publishing Series in Electronic and Optical Materials edited by Katsuaki Suganuma, Woodhead Publishing, 2018, pp. 3-53
ISBN: 978-0-0810-2094-4

Maerz, M.; Eckardt, B.; Wild, M.; Joffe, C.; Zeltner, S.; Endres, S.:
Advanced Vehicle Charging Solutions using SiC and GaN Power Devices
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018, Nuremberg
ISBN 978-3-8007-4646-0

Maerz, M.; Piepenbreier, S.; Kaess, A.:
An Investigation of the Parasitic Impedance on the DC-Link Capacitor of EV Drive Inverters
Proceedings of the 2018 10th International Conference on Integrated Power Electronics Systems (CIPS)
ISBN: 978-3-8007-4540-1

Maerz, M.; Waltrich, U.; Bayer, C.; Zoetl, S.; Tokarski, A.; Zischler, S.; Schletz, A.:
Highly Reliable Power Modules by Pressureless Sintering
Proceedings of the 2018 10th International Conference on Integrated Power Electronics Systems (CIPS)
ISBN: 978-3-8007-4540-1

Maerz, M.; Lorentz, V.; Waller, R.; Waldhoer, S.; Wenger, M.; Gepp, M.; Schwarz, R.; Koffel, S.; Wacker, S.; Akdere, M.; Giegerich, M.:
Power Antifuse Device to Bypass or Turn-off Battery Cells in Safety-Critical and Fail-Operational Systems
Proceedings of the 2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES 2018)
DOI: 10.1109/IESES.2018.8349850

Maerz, M.; Bach, H. L.; Yu, Z.; Letz, S.; Bayer, C.; Waltrich, U.; Schletz, A.:
Vias in DBC Substrates for Embedded Power Modules
Proceedings of the 2018 10th International Conference on Integrated Power Electronics Systems (CIPS)
ISBN: 978-3-8007-4540-1

Matthus, C. D.; Huerner, A.; Erlbacher, T.; Bauer, A. J.; Frey, L.:
Evidence of low injection efficiency for implanted p-emitters in bipolar 4H-SiC high-voltage diodes
Solid-State Electronics Vol. 144, Elsevier, June 2018, pp. 101-105
DOI: 10.1016/j.sse.2018.03.010

Matthus, C. D.; Bauer, A. J.; Frey, L.; Erlbacher, T.:
Wavelength-selective 4H-SiC UV-sensor array
Material Science in Semiconductor Processing, Feb. 2019
DOI: 10.1016/j.mssp.2018.10.019

NAMES AND DATA

CONTINUATION: PUBLICATIONS

Meneghesso, G.; Derluyn, J.; Meissner, E.; Medjdoub, F.; Banerjee, A.; Naundorf, J.; Rittner, M.:
Pushing the limits of GaN-based power devices and power electronics
Bodo´s Power Systems® 8 (2018), pp. 52-55
ISSN: 1863-5598

Morche, C.; Baehr, T.; Ghosh, M.; Kranert, C.; Zimmermann, A.; Franz, H.:
Evaluation of a new hybrid crucible concept for crystallization of mc-silicon ingots
Proceedings of 35th European Photovoltaic Solar Energy Conference and Exhibition (2018), pp. 493-497
DOI: 10.4229/35thEUPVSEC20182018-2AV.1.12

Nouibat, T. H.; Messai, Z.; Chikouch, D.; Ouennoughi, Z.; Rouag, N.; Rommel, M.; Frey, L.:
Normalized differential conductance to study current conduction mechanisms in MOS structures
Microelectronics Reliability, 91, pp. 183-187
DOI: 10.1016/j.microrel.2018.10.001

Onanuga, T.; Kaspar, C.; Sailer, H.; Erdmann, A.:
Accurate determination of 3D PSF and resist effects in grayscale laser lithography
Proceedings of SPIE Advanced Lithography 2018, paper 107750I
DOI: 10.1117/12.2326007

Ortiz, R.; Aurrekoetxea-Rodríguez, I.; Rommel, M.; Quintana, I.; Vivanco, M.; Toca-Herrera, J. L.:
Laser Surface Microstructuring of a Bio-Resorbable Polymer to Anchor Stem Cells, Control Adipocyte Morphology, and Promote Osteogenesis
polymers 10 (2018) 1337
https://doi.org/10.3390/polym10121337

Ott, L.; Han, Y.; Wunder, B.; Bodensteiner, F.; Maerz, M.:
Evaluation of DC-DC-Converter Impedance Passivity using Pseudo-Random Test Signals
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018, Nuremberg
ISBN: 978-3-8007-4646-0

Pai, A.; Reiter, T.; Maerz, M.:
Efficiency Investigation of Full-SiC versus Si-based Automotive Inverter Power Modules at Equal Commutation Speed
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018, Nuremberg
ISBN: 978-3-8007-4646-0

Philipsen, V.; Luong, V.; Opsomer, K.; Hendrickx, E. ; Erdmann, A.; Evanschitzky, P.; van de Kruijs, R.; Heidarnia-Fathabad, Z.; Scholze, F.; Laubis, C.:
Novel EUV mask absorber evaluation in support of next-generation EUV imaging
Proceedings of SPIE Advanced Lithography 2018, paper 108100C
DOI: 10.1117/12.2501799

Piepenbreier, S.; Kaess, A.; Maerz, M.:
An Investigation of the Parasitic Impedance on the DC-Link Capacitor of EV Drive Inverters
IEEE 10th Int. Conference on Integrated Power Electronics Systems (CIPS), Stuttgart, 2018
ISBN: 978-3-8007-4540-1

Purgat, P.; Mackay, L.; Schulz, M.; Han, Y.; Qin, Z.; Maerz, M.; Bauer, P.:
Design of a Power Flow Control Converter for Bipolar Meshed LVDC Distribution Grids
IEEE 18th Int. Power Electronics and Motion Control Conference (PEMC), Budapest
DOI: 10.1109/EPEPEMC.2018.8521853

Rosenberger, M.; Girschikofsky, M.; Förthner, M.; Belle, S.; Rommel, M.; Frey, L.; Schmauss, B.; Hellmann, R.:
TiO2 surface functionalization of COC based planar waveguide Bragg gratings for refractive index sensing
Journal of Optics, Bd. 20, H.1
DOI: 10.1088/2040-8986/aa9bcf

Rosskopf, A. ; Volmering, S. ; Ditze, S. ; Joffe, C. ; Baer, E.:
Autonomous circuit design of a resonant converter (LLC) for on-board chargers using genetic algorithms
Proceedings of IEEE Transportation and Electrification Conference and Expo, ITEC 2018, pp. 96-101
DOI: 10.1109/ITEC.2018.8450100

Rosskopf, A.; Knoerzer, K.; Baer, E.; Ehrlich, S.:
Optimized 2D positioning of windings in inductive components by genetic algorithm
Proceedings of 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2018, pp. 144-149
DOI: 10.1109/EuroSimE.2018.8369881

Scharin-Mehlmann, M.; Haering, A.; Rommel, M.; Dirnecker, T.; Friedrich, O.; Frey, L.; Gilbert, D.:
Nano- and micro-patterned S-, H-, and X-PDMS for cell-based applications: Comparison of wettability, roughness, and cell-derived parameters
Frontiers in Bioengineering and Biotechnology, Bd. 6
DOI: 10.3389/fbioe.2018.00051

NAMES AND DATA

CONTINUATION: PUBLICATIONS

Schellenberger, M.; Roeder, G.; Anger, S.; and Klingert, F.:
"Dr. Production®" and Predictive Maintenance: Lessons Learned from Semiconductor Manufacturing,
Proceedings of the 9th International Conference on "Power Electronics for Plasma Engineering", Freiburg, 2018
ISBN 978-83-930983-8-5

Schoeck, J.; Schlichting, H.; Kallinger, B.; Erlbacher, T.; Rommel, M.; Bauer, A. J.:
Influence of Triangular Defects on the Elecrtical Characteristics of 4H-SiC Devices
Material Science Forum 924 (2018), pp. 164-167
DOI: 10.4028/www.scientific.net/MSF.924.164

Schriefer, T.; Hofmann, M.:
Assessing the vibrational response and robustness of electronic systems by dissolving time and length scale
IEEE 19th Int. Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EurosimE), Toulouse, 2018
DOI: 10.1109/EuroSimE.2018.8369868

Schriefer, T.; Hofmann, M.; Rauh, H.; Eckardt, B.; Maerz, M.:
Parameter study on the electrical contact resistance of axially canted coil springs for high-current systems
64th IEEE Holm Conference on Electrical Contacts, Albuquerque, 2018
DOI: 10.1109/HOLM.2018.8611640

Schriefer, T.; Hofmann, M.; Maerz, M.:
Vibrational resistance investigation of an IGBT gate driver utilizing Frequency Response Analysis (FRA) and Highly Accelerated Life Test (HALT)
IEEE 10th Int. Conference on Integrated Power Electronics Systems (CIPS), Stuttgart, 2018
ISBN: 978-3-8007-4540-1

Schrüfer, D.; Ellinger, M.; Jank, M.; Frey, L.; Weigel, R.; Hagelauer, A.:
Circuits with Scaled Metal Oxide Technology for Future TOLAE RF Systems
Proceedings of the 48th European Microwave Conference, pp. 737-740
ISBN: 978-2-87487-051-4

Schultheiss, F.; Thinh, N. - X.; Endruschat, A.; Maerz, M.:
Minimum Volume Design of a Forced-Air Cooled Three-Phase Power Factor Correction Stage for Electric Vehicle Chargers
IEEE Transportation Electrification Conference (ITEC) 2018, Long Beach, CA
DOI: 10.1109/ITEC.2018.8450111

Shapouri Ghazvini, M.; Pulletikurthi, G.; Cuia, T.; Kuhl, C.; Endres, F.:
Electrodeposition of zinc from 1-ethyl-3-methylimidazolium acetate-water mixtures: Investigations on the applicability of the electrolyte for Zn-air batteries
Journal of The Electrochemical Society 165 (9) (2018) D354-D363
DOI: 10.1149/2.0181809jes

Shen, L.; Mueller, S.; Cheng, X.; Zhang, D.; Zheng, L.; Xu, D.; Yu, Y.; Meissner, E.; Erlbacher, T.:
The GaN trench gate MOSFET with floating islands: High breakdown voltage and improved BFOM
Superlattices and Microstructures, Volume 114, February 2018, pp. 200-206
DOI: 10.1016/j.spmi.2017.12.033

Steinberger, M.: Geiling, J.; Oechsner, R.; Frey, L.:
Anode recirculation and purge strategies for PEM fuel cell operation with diluted hydrogen feed gas
Applied Energy, 232, pp. 572-582
DOI: 10.1016/j.apenergy.2018.10.004

Stockmeier, L.; Kranert, C.; Raming, G.; Miller, A.; Reimann, C.; Rudolph, P.; Friedrich, J.:
Edge facet dynamics during the growth of heavily doped n-type silicon by the Czochralski-method
Journal of Crystal Growth 491 (2018), pp. 57-65
DOI: 10.1016/j.jcrysgro.2018.03.028

Stolzke, T.; Dirnecker, T.; Schwarz, J.; Frey, L.:
Investigation of magnetic properties from a manganese–zinc–ferrite polymer bonded material
International Journal of Applied Electromagnetics and Mechanics, pp. 1-8
DOI: 10.3233/JAE-171244

Stumpf, F.; Abu Quba, A.A.; Singer, P.; Rumler, M.; Cherkashin, N.; Schamm-Chardon, S.; Cours, R.; Rommel, M.:
Detailed characterisation of focused ion beam induced lateral damage on silicon carbide samples by electrical scanning probe microscopy and transmission electron microscopy
Journal of Applied Physics 123 (2018) 125104
https://doi.org/10.1063/1.5022558

Trempa, M.; Müller, G.; Friedrich, J.; Reimann, C.:
Grain boundaries in multicrystalline silicon
in Handbook of Photovoltaic Silicon (Ed. D. Yang), Springer, Berlin (2018), pp. 1-48
DOI: https://doi.org/10.1007/978-3-662-52735-1

NAMES AND DATA

CONTINUATION: PUBLICATIONS

Waltrich, U.; Bayer, C. F.; Zoetl, S.; Tokarski, A.; Zischler, S.; Schletz, A.; Maerz, M.:
Highly Reliable Power Modules by Pressureless Sintering
10th Int. Conference on Integrated Power Electronics Systems (CIPS) 2018, pp. 547-551
ISBN: 978-3-8007-4540-1

Weisse, J.; Hauck, M.; Sledziewski, T.; Tschiesche, M.; Krieger, M.; Bauer, A. J.; Mitlehner, H.; Frey, L.; Erlbacher, T.:
Analysis of Compensation Effects in Aluminum-Implanted 4H-SiC Devices
Material Science Forum 924 (2018), pp. 184-187
DOI: 10.4028/www.scientific.net/MSF.924.184

Woldeamanual, D.S.; Erdmann, A.; Maier, A.:
Application of deep learning algorithms for lithographic mask characterization
Proceedings of SPIE Advanced Lithography 2018, paper 1069408
DOI: 10.1117/12.2312478

Xu, Z.; He, Z.; Song, Y.; Fu, X.; Rommel, M.; Luo, X.; Hartmaier, A.; Zhang, J.; Fang, F.:
Topic Review: Application of Raman Spectroscopy Characterization in Micro/Nano-machining
Micromachines 9 (2018) 361
https://doi.org/10.3390/mi9070361

Yu, Z.; Zeltner, S.; Boettcher, N.; Rattmann, G.; Leib, J.; Bayer, C. F.; Schletz, A.; Erlbacher, T.; Frey, L.:
Heterogeneous Integration of Vertical GaN Power Transistor on Si Capacitor for DC-DC Converters
Conference Paper, ESTC Dresden, September 18, 2018
DOI: 10.1109/ESTC.2018.8546362

Zoerner, A.; Oertel, S.; Jank, M.; Frey, L.; Langenstein, B.; Bertsch, T.:
Human Sweat Analysis Using a Portable Device Based on a Screen-printed Electrolyte Sensor
Electroanalysis, Bd. 30, H. 4
DOI: 10.1002/elan.201700672

PRESENTATIONS

Amat, E.; Kluepfel, F.; del Moral, A.; Bausells, J.; Perez-Murano, F.:
Impact of quantum dot characteristics on the hybrid SET-FET circuit behavior
50th International Conference of Solid-State Devices and Materials
Tokyo, Japan, September 10 - 14, 2018

Amat, E.; Kluepfel, F.; del Moral, A.; Bausells, J.; Perez-Murano, F.:
Quantum dot location relevance into SET-FET circuits based on FinFET devices
33rd Conference on Design of Circuits and Integrated systems
Lyon, France, November 14 - 16, 2018

Bach, H. L.; Endres, T.; Dirksen, D.; Zischler, S.; Bayer, C. F.; Schletz, A.; Maerz, M.:
Ceramic Embedding as Packaging Solution for Future Power Electronic Applications
Int. Power Electronics Conference (ECCE IPEC) 2018
Niigata, Japan, May 20 - 24, 2018

Bach, H. L.; Yu, Z.; Letz, S.; Bayer, C. F.; Waltrich, U.; Schletz, A.; Maerz, M.:
Vias in DBC Substrates for Embedded Power Modules
CIPS 2018, 10th International Conference on Integrated Power Electronics Systems
Stuttgart, Germany, March 20 - 22, 2018

Baehr, T.; Ghosh, M.; Kranert, C.; Reimann, C.; Morche, C.:
Development of methods for reducing the red zone in the top region of mc-silicon ingots
35th European Photovoltaic Solar Energy Conference (35th EU PVSEC)
Brussels, Belgium, September 24 - 28, 2018

Baer, E.:
Simulation of layer profiles and deposition rates for physical vapor deposition processes
GMM Workshop "New Developments in Deposition and Etching", Fraunhofer IISB
Erlangen, Germany, December 5, 2018

Baer, E.; Lorenz, J.:
The effect of etching and deposition processes on the width of spacers created during self-aligned double patterning
Conference on Simulation of Semiconductor Processes and Devices 2018 (SISPAD 2018)
Austin, USA, September 24 - 26, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Bauer, A. J.:
Advanced Gate Oxides on 4H-SiC Formed at High Temperature and Low Oxygen Partial Pressure
SiC 2018, The 2nd International Symposium on SiC Materials and Devices 2018
Nurimaru APEC House, Busan, Korea, November 29, 2018

Bauer, A. J.:
Forming advanced gate oxides on 4H-SiC by increasing oxidation temperature and concurrent oxygen partial pressure reduction
20th Workshop on Dielectrics in Microelectronics
Park Inn Alexander Platz, Berlin, Germany, June 11 - 14, 2018

Bauer, A. J.:
O2 partial pressure reduction at high oxidation temperature for advanced 4H-SiC gate oxides
43. Treffen der GMM Fachgruppe Heißprozesse und RTP
Fraunhofer IISB, Erlangen, Germany, April 11, 2018

Bauer, A. J.:
SiC Activities
17. Treffen der GMM-Fachgruppe 1.2.6 "Prozesskontrolle, Inspektion & Analytik"
Fraunhofer IISB, Erlangen, Germany, March 15, 2018

Bayer, C. F.:
Electrochemical Corrosion in Power Modules due to Harsh Environments
Semicon West
San Francisco, USA, July 9 - 12, 2018

Bayer, C. F.:
FEM-Simulation in Designing new Power Modules
Semicon West
San Francisco, USA, July 9 - 12, 2018

Bayer, C. F.:
Korrosion in leistungselektronischen Modulen
Vortrag GMM-Fachgruppe 1.2.6 „Prozesskontrolle, Inspektion & Analytik"
Erlangen, Germany, March 15, 2018

Bayer, C. F.:
Power Electronics Packaging at Fraunhofer IISB – Double Sided Cooling, Ceramic Embedding, and more
Semicon West
San Francisco, USA, July 9 - 12, 2018

Bayer, C. F.; Diepgen, A.; Filippi, T.; Fuchs, C.; Wuestefeld, S.; Kellner, S.; Waltrich, U.; Schletz, A.:
Electrochemical Corrosion on Ceramic Substrates for Power Electronics - Causes, Phenomenological Description, and Outlook
CIPS 2018, 10th International Conference on Integrated Power Electronics Systems
Stuttgart, Germany, March 20 - 22, 2018

Beier, M.; Reimann, C.; Friedrich, J,; Peuker, U.; Leißner, T.; Groeschel, M.; Ischenko, V.:
Silicon waste from the photovoltaic industry – a material source for the next generation battery technology?
International Workshop E-Mobility & Circular Economy
Freiberg, Germany, June 6 - 7, 2018

Belete, Z.; Baer, E.; Erdmann, A.:
Modeling of block copolymer dry etching for directed self-assembly lithography
SPIE Advanced Lithography
San Jose, USA, February 25 - March 1, 2018

Besendoerfer, S.:
Defects in III-nitrides – Dislocations in GaN-on-Si for power HEMTs
Scientific Colloquium of Mie University
Mie, Japan, November 20, 2018

Besendoerfer, S.:
Defects in III-nitrides – Dislocations in GaN-on-Si for power HEMTs
Scientific Colloquium of Nagoya University
Nagoya, Japan, November 21, 2018

Besendoerfer, S.; Meissner, E.; Friedrich, J.:
Microstructural features leading to large vertical leakage spots in GaN-on-Si HEMT structures
10th International Workshop on Nitride Semiconductors (IWN 2018)
Kanazawa, Japan, November 11 - 16, 2018

Dresel, F.; Tham, N.; Erlbacher, T.; Schletz, A.:
Lifetime Testing Method for Ceramic Capacitors for Power Electronics Applications
CIPS 2018, 10th International Conference on Integrated Power Electronics Systems
Stuttgart, Germany, March 20 - 22, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Dresel, F.; Letz, S.; Zischler, S.; Schletz, A.; Novak, M.:
Selective silver sintering of semiconductor dies on PCB
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018
Nuremberg, Germany, June 5 - 7, 2018

Eckardt, B.; Wild, M.; Joffe, C.; Zeltner, S.; Endres, S.; Maerz, M.:
Advanced Vehicle Charging Solutions Using SiC and GaN Power Devices
Int. Conference on Power Conversion and Intelligent Motion (PCIM) 2018
Nuremberg, Germany, June 5 - 7, 2018

Epelbaum, B.; Mueller, S.; Besendoerfer, S.; Meissner, E.; Friedrich, J.:
Bulk AlN crystals grown in different crucible materials
DGKK-Arbeitskreis Halbleiterkristalle
Erlangen, Germany, October 10, 2018

Epelbaum, B.; Mueller, S.; Besendoerfer, S.; Meissner, E.; Friedrich, J.:
Morphological stability of growth facets in bulk AlN crystals grown in different crucible materials
1st German-Austrian Conference on Crystal Growth (GACCG/DKT2018)
Vienna, Austria, February 14 - 16, 2018

Erdmann, A.:
Mask and illumination induced imaging effects in EUV lithography
European Optical Society Biennial Meeting (EOSAM)
Delft, Netherlands, October 2018

Erdmann, A.:
Optical and material-driven resolution enhancements for semiconductor lithography
European Optical Society Biennial Meeting (EOSAM)
Delft, Netherlands, October 2018

Erdmann, A.:
Understanding and optimization of imaging for EUV lithography
11th International Conference on Optics-photonics Design & Fabrication (ODF)
Hiroshima, Japan, November 2018

Erdmann, A.; Evanschitzky, P.; Bottiglieri, G.; van Setten, E.; Fliervoet, T.:
3D mask effects in high NA EUV imaging
16th Lithography Simulation Workshop of the IISB
Gräfenberg, Germany, September 13 -15, 2018

Erdmann, A.; Evanschitzky, P.; Mezilhy, H.; Philipsen, V.; Hendrickx, E.; Bauer, M.:
Attenuated PSM for EUV: Can they mitigate 3D mask effects?
SPIE Advanced Lithography
San Jose, USA, February 25 - March 1, 2018

Erlekampf, J.; Kallinger, B.; Berwian, P.; Friedrich, J.; Frey, L.:
Impact of substrate quality on the minority carrier lifetime in 4H-SiC during epitaxial growth and post-epi processing
12th European Conference on Silicon Carbide and Related Materials (ECSCRM 2018)
Birmingham, UK, September 2 - 6, 2018

Erlekampf, J.; Kallinger, B.; Berwian, P.; Friedrich, J.:
Impact of substrate quality on the minority carrier lifetime in 4H-SiC during epitaxial growth and post-epi processing
DGKK-Arbeitskreis Halbleiterkristalle
October 10, 2018, Erlangen, Germany

Erlekampf, J.; Kaminzky, D.; Kallinger, B.; Berwian, P.; Friedrich, J.:
Minority carrier lifetime improvement in n-type 4H-SiC by nitrogen ion implantation
1st German-Austrian Conference on Crystal Growth (GACCG/DKT2018)
Vienna, Austria, February 14 - 16, 2018

Erlekampf, J.; Kallinger, B.; Berwian, P.; Friedrich, J.; Frey, L.:
Principle of lifetime-engineering in 4H-SiC by ion implantation
12th European Conference on Silicon Carbide and Related Materials (ECSCRM 2018)
Birmingham, UK, September 2 - 6, 2018

Faraji, S.; Schroeter, C.; Meissner, E.; Friedrich, J.:
GaN seed layers grown by MOVPE for the purpose of GaN self-separation from sapphire substrate in HVPE
1st German-Austrian Conference on Crystal Growth (GACCG/DKT2018)
Vienna, Austria, February 14 - 16, 2018

Friedrich, J.:
Wide Band Gap Semiconductor Materials - Status and Challenges
Strategic Materials Conference, Semicon Europa
Munich, Germany, November 11 - 13, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Friedrich, J.; Jung, T.; Denisov, A.; Muehe, A.; Seebeck, J.:
Limitations of the growth rate during pulling of large diameter silicon crystals by the Czochralski technique
DGKK-Arbeitskreis Halbleiterkristalle
Erlangen, Germany, October 10, 2018

Friedrich, J.; Jung, T.; Mosel, F.; Muehe, A.; Seebeck, J.:
Limitations of the growth rate during pulling of large diameter silicon crystals by the Czochralski technique
9th International Workshop on Modeling in Crystal Growth
Big Island, Hawaii, October, 21 - 24, 2018

Gerstner, H.; Endruschat, A.; Heckel, T.; Joffe, C.; Eckardt, B.; Maerz, M.:
Non-linear Input Capacitance Determination of WBG Power FETs using Gate Charge Measurements
WiPDA 2018, IEEE 6th Workshop on Wide Bandgap Power Devices and Applications
Atlanta, USA, October 31 - November 2, 2018

Gosses, K.; Kaiser, J.; Ott, L.; Schulz, M.; Fersterra, F.; Wunder, B.; Han, Y.; Lavery, M.; Maerz, M.:
Fault Considerations of Non-Isolated Electric Vehicle Chargers with a Mutual DC Supply
ITEC 2018, IEEE Transportation Electrification Conference
Long Beach, USA, June 13 - 15, 2018

Govalkar, P.; Syben, C.; Erdmann, A.; Maier, A.:
A generalized framework for reconstructing low-resolution lithography images using Fourier ptychography and U-net convolutional network
16th Lithography Simulation Workshop of the IISB
Gräfenberg, Germany, September 13 -15, 2018

Haeublein, V.:
Energetische Kontamination bei der Al-Implantation
59. Treffen der GMM-Fachgruppe 1.2.2 "Ionenimplantation"
Fraunhofer IISB, Erlangen, Germany, April 12, 2018

Haeublein, V.; Bauer, A.; Ryssel, H.; Frey, L.:
Mass Separation Issues for the Implantation of Doubly Charged Aluminum Ions
22nd International Conference on Ion Implantation Technology (IIT 2018)
Würzburg, Germany, September 16 - 21, 2018

He, R.; Heyn, W.; Thiel, F.; Reimann, C.; Beier, M.; Friedrich, J.; Schierning, G.; Nielsch, K.:
Turning waste into profit: the potential of Si slurry for high temperature thermoelectric applications
Materials Science and Engineering Congress (MSE)
Darmstadt, Germany, September 26 - 28, 2018

Heinig, K.H.; von Borany, J.; Stegemann, K.H.; Prüfer, T.; Xu, X.; Moeller, W.; Gharbi, A.; Tiron, R.; Kluepfel, F.; Hlawacek, G.; Bischoff, L.; Engelmann, H.-J.; Facsko, S.:
Manufacturability of single Si quantum dots for single electron transistors operating at room temperature
EMRS Fall Meeting, Symp. K: Nanomaterials – electronics & photonics
Warsaw, Poland, September 17 - 20, 2018

Hutzler, A.; Matthus, C. D.; Dolle, C.; Rommel, M.; Jank, M.; Spiecker, E.; Frey, L.:
Large-Area Layer Counting of 2D Materials via Visible Reflection Spectroscopy
IMC19, 19th International Microscopy Congress
Sydney, Australia, September 9 - 14, 2018

Hutzler, A.; Matthus, C. D.; Rommel, M.; Dolle, C.; Jank, M.; Frey, L.; Spiecker, E.:
Optical methods for layer counting of 2D materials
GMM Workshop der Fachgruppe „Prozesskontrolle, Inspektion & Analytik", Thema: „Materialanalytik in der Halbleitertechnologie"
FhG IISB, Erlangen, Germany, March 15, 2018

Ismail, M.; Evanschitzky, P.; Erdmann, A.; Bottiglieri, G.; van Setten, E.; Fliervoet, T.:
Simulation study of illumination effects in high-NA EUV lithography
SPIE Optical Systems Design
Frankfurt, Germany, May 2018

Jank, M.:
Dünnschichtelektronik und –sensorik für großflächige Anwendungen
Kooperationsforum Interieur im Automobil – Enabling Technologies, Bayern Innovativ
Bamberg, Germany, March 14, 2018

Jank, M.:
Future Materials and Hazards, Novel Materials and Nano-Risk in Semiconductor Industry
Öffentlicher Workshop des EU-Projekts NanoStreeM im Rahmen der SEMICON Europa
München, Germany, November 14, 2019

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Jank, M.:
Future Materials and the risk assessment framework
NanoStreeM Project Webinar, Nanoelectronics Industry Association (NIA), https://www.youtube.com/watch?v=sLXtasKAC0I
December, 6, 2018

Jank, M.; Oertel, S.:
Gedruckte Elektrolytsensoren für Fitness-Anwendungen, Printed Electronics für Mobility und Life Sciences
FAPS-IPC
Nürnberg, Germany, July 04 - 05, 2018

Jauß, T.; Danilewsky, A.; Sorgenfrei, T.; Reimann, C.; Friedrich, J.:
Synchrotron white beam x-ray topography investigation of particle incorporation in silicon
1st German-Austrian Conference on Crystal Growth (GACCG/DKT2018)
Vienna, Austria, February 14 - 16, 2018

Johnsson, A.; Pichler, P.; Schmidt, G.; Hauf, M.; Niedernostheide, F.J.:
Platinum in silicon after post-implantation annealing: From experiments to process and device modelling
22nd International Conference on Ion Implantation Technology (IIT 2018)
Würzburg, Germany, September 16 - 21, 2018

Kaiser, J.; Schork, F.; Gosses, K.; Han, Y.; Schulz, M.; Ott, L.; Wunder, B.; Maerz, M.:
Converter Overvoltage Protection for DC-Grids
INTELEC 2018, International Telecommunications Engery Conference
Torino, Italy, October 7 - 11, 2018

Kallinger, B.:
Defects and minority carrier lifetime in 4H-SiC
Physical Colloquium, Friedrich-Alexander-University Erlangen-Nuremberg
Erlangen, Germany, June 11, 2018

Kallinger, B.; Erlekampf, J.; Rommel, M.; Berwian, P.; Friedrich, J.; Matthus, C. D.:
Defects and carrier lifetime in 4H-SiC
Symposium R, New frontiers in wide-bandgap semiconductors and heterostructures for electronics, optoelectronics and sensing
E-MRS Fall Meeting
Warsaw, Poland, September 17 - 20, 2018

Kallinger, B.; Erlekampf, J.; Roßhirt, K.; Berwian, P.; Stockmeier, M.; Vogel, M.; Hens, P.; Wischmeyer, F.:
Influence of substrate properties on the defectivity and minority carrier lifetime in 4H-SiC homoepitaxial layers
12th European Conference on Silicon Carbide and Related Materials (ECSCRM 2018)
Birmingham, UK, September 2 - 6, 2018

Klingert, F.:
Failure Prediction of Equipment Operator Influences in Mass Manufacturing at Infineon
Predictive Analytics World (PAW) for Industry 4.0 Conference 2018
Munich, Germany, May 6 - 7, 2018

Kluepfel, F.:
Single-electron transistors: fabrication and modeling
IISB/LEB Colloquium, Fraunhofer IISB
Erlangen, Germany, December 3, 2018

Kluepfel, F.:
Single electron transistors: fabrication and modeling within the project IONS4SET
Seminar "Grundlagen und Anwendungen moderner Halbleiterstrukturen", Felix Bloch Institute for Solid State Physics
Leipzig, Germany, July 4, 2018

Kocher, M.; Erlbacher, T.; Rommel, M.; Bauer, A.J.:
Decoration of Al implantation profiles in 4H-SiC by bevel grinding and dry oxidation,
ECSCRM 2018, 12th European Conference on Silicon Carbide & Related Materials
Birmingham, UK, September 2 - 6, 2018

Kocher, M.; Yao, B.; Weisse, J.; Rommel, M.; Xu, Z.W.; Erlbacher, T.; Bauer, A.J.:
Determination of compensation ratios of Al-implanted 4H-SiC by TCAD modelling of TLM measurements
ECSCRM 2018, 12th European Conference on Silicon Carbide & Related Materials
Birmingham, UK, September 2 - 6, 2018

Kocher, M.; Rommel, M.; Sledziewski, T.; Haeublein, V.; Bauer, A.J.:
Dose dependent profile deviation of implanted aluminum in 4H-SiC during high temperature annealing
IIT 2018, 22nd International Conference on Ion Implantation Technology
Würzburg, Germany, September 16 - 21, 2018

Kreutzer, O.; Billmann, M.; Gerner, M.; Maerz, M.:
A 3.6 kV full SiC fuel cell boost converter for high power electric aircraft
ITEC 2018, IEEE Transportation Electrification Conference
Long Beach, USA, June 13 - 15, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Kreutzer, O.; Billmann, M.; Maerz, M.:
Is an antiparallel SiC-Schottky diode necessary - Calorimetric Analysis of SiC-MOSFETs switching behavior
PCIM Europe 2018, International Exhibition and Conference for Power Electronic, Intelligent Motion, Renewable Energy and Energy Management
Nuremberg, Germany, June 5 - 7, 2018

Kupka, I.; Schmidtner, L.; Trempa, M.; Reimann, C.; Friedrich, J.:
Influence of process parameter on the bubble formation in fused silica crucibles during Czochralski growth of mono-crystalline silicon for solar cell application
10th International Workshop on Crystalline Silicon for Solar Cells CSSC-10
Sendai, Japan, April 8 - 11, 2018

Kupka, I.; Schmidtner, L.; Trempa, M.; Reimann, C.; Friedrich, J.:
Influence of process parameter on the bubble formation in fused silica crucibles during Czochralski growth of mono-crystalline silicon for solar cell application
35th European Photovoltaic Solar Energy Conference (EU PVSEC)
Brussels, Belgium, September 24 - 28, 2018

Lehninger, D.; Rafaja, D.; Wünsche, J.; Schneider, F.; von Borany, J.; Heitmann, J.:
Stabilization of orthorhombic (Zr,Ta)O2 in thin Zr-Ta-O films
20th Workshop on Dielectrics in Microelectronics
Berlin, Germany, June 10 - 14, 2018

Lenahan, F.; Evanschitzky, P.; Philipsen, V.; Erdmann, A.:
Rigorous EUV SRAF optimization
16th Lithography Simulation Workshop of the IISB
Gräfenberg, Germany, September 13 -15, 2018

Letz, S.; Farooghian, A.; Simon, F. B.; Schletz, A.:
Modeling the rate-dependent inelastic deformation of porous polycrystalline silver films
ESREF 2018
Aalborg, Denmark, October 1 - 5, 2018

Lorentz, V. R. H; Waller, R.; Waldhoer, S.; Wenger, M.; Gepp, M.; Schwarz, R.; Koffel, S.; Wacker, S.; Akdere, M.; Giegerich, M.; Maerz, M.:
Power Antifuse Device to Bypass or Turn-off Battery Cells in Safety-Critical and Fail-Operational Systems
IEEE Int. Conference on Industrial Electronics for Sustainable Energy Systems (IESES 2018)
Hamilton, New Zealand, January 30 - February 2, 2018

Lorenz, J.:
SUPERAID7 – Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm Node
Two posters presented at the European Forum for Electronic Components and Systems (EFECS)
Lisbon, Portugal, November 20 - 22, 2018

Lorenz, J.; Asenov, A.; Bär, E.; Barraud, S.; Millar, C.; Nedjalkov, M.:
Process variability for devices at and beyond the 7 nm node
233rd Meeting of the Electrochemical Society (ECS Spring Meeting 2018)
Seattle, USA, May 13 -17, 2018

Meissner, E.:
The effects of structural disturbances on the electrical behavior of GaN from a materials perspective
Scientific seminar of Ferdinand Braun Institute
Berlin, Germany, February 16, 2018

Meissner, E.; Besendoerfer, S.; Friedrich, J.:
Possibilities and challenges in the investigation of materials defects and their influence on GaN devices
10th International Workshop on Nitride Semiconductors (IWN 2018)
Kanazawa, Japan, November 11 - 16, 2018

Morche, C.; Baehr, T.; Ghosh, M.; Kranert, C.; Zimmermann, A.; Franz, H.:
Evaluation of a new hybrid crucible concept for crystallization of mc-silicon ingots
35th European Photovoltaic Solar Energy Conference (35th EU PVSEC)
Brussels, Belgium, September 24 - 28, 2018

Oertel, S.; Zoerner, A.; Jank, M.; Lang, N.:
Screen-printed Sensors for Sweat
Analysis in Sports Wearables, Printed Electronics Europe
Berlin, Germany, May 11, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Onanuga, T.; Kaspar, C.; Sailer, H.; Erdmann, A.:
Accurate determination of 3D PSF and resist effects in grayscale laser lithography
34th European Mask and Lithography Conference
Grenoble, France, June 2018

Ott, L.:
Stabilität im DC-Smart Grid
Technologieseminar DC-Smart Grid – Netz- und Energiemanagement in der Produktion
Stuttgart, Germany, June 7, 2018

Ott, L.; Han, Y.; Wunder, B.; Bodensteiner, F.; Maerz, M.:
Evaluation of DC-DC-Converter Impedance Passivity using Pseudo-Random Test Signals
PCIM Europe 2018, International Exhibition and Conference for Power Electronic, Intelligent Motion, Renewable Energy and Energy Management
Nuremberg, Germany, June 5 - 7, 2018

Pai, A.; Reiter, T.; Maerz, M.:
Efficiency Investigation of Full-SiC versus Si-based Automotive Inverter Power Modules at Equal Commutation Speed
PCIM Europe 2018, International Exhibition and Conference for Power Electronic, Intelligent Motion, Renewable Energy and Energy Management
Nuremberg, Germany, June 5 - 7, 2018

Philipsen, V.; Luong, V.; Opsomer, K.; Hendrickx, E. ; Erdmann, A.; Evanschitzky, P.; van de Kruijs, R.; Heidarnia-Fathabad, Z.; Scholze, F.; Laubis, C.:
Novel EUV mask absorber evaluation in support of next-generation EUV imaging
SPIE EUV Lithography
Monterey, USA, September 2018

Pichler, P.; Sledziewski, T.; Haeublein, V.; Bauer, A.J.; Erlbacher, T.:
Channeling in 4H-SiC from an application point of view
European Conference on Silicon Carbide and Related Materials (ECSCRM 2018)
Birmingham, UK, September 2 - 6, 2018

Purgat, P.; Mackay, L.; Schulz, M.; Han, Y.; Qin, Z.; Maerz, M.; Bauer, P.:
Design of a Power Flow Control Converter for Bipolar Meshed LVDC Distribution Grids
IEEE-PEMC, 18th International Conference on Power Electronics and Motion Control
Budapest, Hungary, August 26 - 30, 2018

Reimann, C.; Trempa, M.; Schwanke, S.; Sturm, F.; Kupka, I.; Schenk, C.; Weizhi, L.; Friedrich, J.:
Effect of commercially available SiO2 diffusion barriers on the material quality of directionally solidified high performance multi-crystalline silicon ingots
SNEC, 12th International Photovoltaic Power Generation and Smart Energy Conference & Exhibition
Shanghai, China, May 28 - 30, 2018

Roeder, G.; Meyer, M.; Jacob, S.; Fal, Y.; Schellenberger, M.:
Towards Cognitive Power Electronics 4.0 - First Results of a Demonstrator for Pump Monitoring
21. Workshop der GMM – Fachgruppe 1.2.3 Abscheide- und Ätzverfahren
Erlangen, Germany, December 5, 2018

Rosskopf, A.; Baer, E.; Schuster, S.; Lippert. O.
Calculation of litz wire losses with the PEEC method using a geometry-based extraction of dominating mutual instances
IEEE Conference on Electromagnetic Field Computation (CEFC 2018)
China, October 28 - 31, 2018

Schellenberger, M.:
Cognitive Power Electronics 4.0: Auf dem Weg zur „intelligenten" Leistungselektronik
Cluster-Seminar: Zustandsüberwachung von elektronischen Systemen und Produktionsanlagen, Methoden und Technologien
Nürnberg, Germany, October 11, 2018

Schellenberger, M.:
Dr. Production und Cognitive Power Electronics – Aktuelle Forschung für Predictive Maintenance
VDMA-Workshop „Predictive Maintenance - ganz anschaulich"
Fraunhofer IISB, Erlangen, Germany, May 16, 2018

Schellenberger, M.:
Predictive Maintenance: Lessons learned from Semiconductor Manufacturing
MAPEtronica – Conference about Industry 4.0
TH Ingolstadt, Germany, January 12, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

Schellenberger, M.:
Predictive Probing: A novel approach to minimize efforts at final test
SEMICON Europa 2018, TechARENA: Metrology for Emerging Technologies
Munich, Germany, October 13 - 16, 2018

Schletz, A.:
Herausforderungen durch hohe Leistungsdichte (hohe Temperaturen) bei integrierten Systemen
Anwendertraining zur Wide-Bandgap Systemintegration
Bremen, Germany, June 25 - 26, 2018

Schletz, A.:
Power Interconnect Trends
Customer Day 2018, Schweizer Electronic AG
Schramberg, Germany, June 27 - 28, 2018

Schletz, A.:
State of the Art Packaging
Anwendertraining zur Wide-Bandgap Systemintegration
Bremen, Germany, June 25 - 26, 2018

Schletz, A.:
Testen von WBG-Bauelementen II (Fokus: Aufbau- & Verbindungstechnik)
Anwendertraining zur Wide-Bandgap Systemintegration
Bremen, Germany, June 25 - 26, 2018

Schriefer T.:
Bewertung der Betriebsfestigkeit leistungselektronischer Systeme bei hochzyklischer Eingangslast unter Einsatz der Laser-Doppler-Vibrometrie
15. Vibrometer Anwenderkonferenz
Waldbronn, Germany, November 13, 2018

Schriefer T.:
Integration of power electronic systems in harsh environments
E-Motive Expertenforum
Stuttgart, Germany, September 13, 2018

Schriefer, T.:
Untersuchungen zu Hochstromkontakten in integrierten elektrischen Fahrzeugantrieben
12. Anwenderkongress Steckverbinder
Würzburg, Germany, April 4, 2018

Schriefer, T.; Hofmann, M.:
Assessing the vibrational response and robustness of electronic systems by dissolving time and length scale
IEEE 19th Int. Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EurosimE)
Toulouse, France, April 15 - 18, 2018

Schriefer, T.; Hofmann, M.; Rauh, H.; Eckardt, B.; März, M.:
Parameter study on the electrical contact resistance of axially canted coil springs for high-current systems
64th IEEE Holm Conference on Electrical Contacts
Albuquerque, USA, October 14 - 18, 2018

Schultheiss, F.; Thinh, N. - X.; Endruschat, A.; Maerz, M.:
Minimum Volume Design of a Forced-Air Cooled Three-Phase Power Factor Correction Stage for Electric Vehicle Chargers
ITEC 2018, IEEE Transportation Electrification Conference
Long Beach, USA, June 13 - 15, 2018

Schwanke, S.; Reimann, C.; Kuczynski, M.; Hoislbauer, C.; Sans, J.; Friedrich, J.:
Influencing the incorporation of oxygen during the directional solidification of multi-crystalline silicon by adjusting the silicon nitride coating
10th International Workshop on Crystalline Silicon for Solar Cells CSSC-10
Sendai, Japan, April 8 - 11, 2018

Schwanke, S.; Reimann, C.; Kuczynski, M.; Hoislbauer, C.; Sans, J.; Friedrich, J.:
Influencing the incorporation of oxygen during the directional solidification of multi-crystalline silicon by adjusting the silicon nitride coating
35th European Photovoltaic Solar Energy Conference (35th EU PVSEC)
Brussels, Belgium, September 24 - 28, 2018

Seebeck, J.; Kallinger, B.; Meissner, E.; Schröter, C.; Friedrich, J.:
Numerical modelling for epitaxy of wide bandgap semiconductors
9th International Workshop on Modeling in Crystal Growth
Big Island, Hawaii, October, 21 - 24, 2018

NAMES AND DATA

CONTINUATION: PRESENTATIONS

D'Silva, S.; Mülders, T.; Stock, H.J.; Erdmann, A.:
Analysis of resist deformation and shrinkage during lithographic processing
16th Lithography Simulation Workshop of the IISB
Gräfenberg, Germany, September 2018

Simon F. - B.; Letz S.; Schletz, A.:
Influence of the pulse length and temperature swing on the relative lifetime estimation for sintered/soldered chip-on-substrate samples
ESREF 2018
Aalborg, Denmark, October 1 - 5, 2018

Stockmeier, L.; Kranert, C.; Raming, G.; Miller, A.; Reimann, C.; Rudolph, P.; Friedrich, J.:
Edge facet dynamics during the growth of heavily doped n-type silicon by the Czochralski-method
1st German-Austrian Conference on Crystal Growth (GACCG/DKT2018)
Vienna, Austria, February 14 - 16, 2018

Sturm, F.; Reimann, C.; Trempa, M.; Schwanke, S.; Kupka, I.; Schenk, C.; Weizhi, L.; Friedrich, J.:
Effect of commercially available SiO2 diffusion barriers on the material quality of directionally solidified high performance multi-crystalline silicon ingots
35th European Photovoltaic Solar Energy Conference (35th EU PVSEC)
Brussels, Belgium, September 24 - 28, 2018

Trempa, M.; Schwanke, S.; Sturm, F.; Kupka, I.; Reimann, C.; Friedrich, J.:
Role of crucible material and functional diffusion barrier coatings on the material quality of directionally solidified silicon ingots
10th International Workshop on Crystalline Silicon for Solar Cells CSSC-10
Sendai, Japan, April 8 - 11, 2018

Waltrich, U.; Bayer, C. F.; Zötl, S.; Tokarski, A.; Zischler, S.; Schletz, A.; März, M.:
Highly Reliable Power Modules by Pressureless Sintering
CIPS 2018, 10th International Conference on Integrated Power Electronics Systems
Stuttgart, Germany, March 20 - 22, 2018

Wang, K.; Friedrich, J.; Jung, T.; Seebeck, J.; Derby, J. J.:
A lumped-parameter model for oxygen segregation transport in Czochralski crystal growth
9th International Workshop on Modeling in Crystal Growth
Big Island, Hawaii, October, 21 - 24, 2018

Weisse, J.; Csato, C.; Rommel, M.; Erlekampf, J.; Rüb, M.; Akhmadaliev, S.; Mitlehner, H.; Bauer, A. J.; Häublein, V.; Frey, L.; Erlbacher, T.:
Impact of Al-ion implantation on the formation of deep defects in n-type 4H-SiC
22nd International Conference on Ion Implantation Technology (IIT 2018)
Würzburg, Germany, September 16 - 21, 2018

Woldeamanual, D.S.; Erdmann, A. ; Maier, A.:
Application of deep learning algorithms for lithographic mask characterization
SPIE Optical Systems Design
Frankfurt, Germany, May 2018

Wunder, B.:
Ladetechniken für Elektrofahrzeuge
Technikerschule Bayreuth
Bayreuth, Germany, February 1, 2018

Xu, Z.; Zhao, J.; Djurabekova, F.; Rommel, M.; Nordlung, K.:
Defect functional structures of 4H-SiC and diamond induced by ion implantation: MD simulation and spectral characterization
COSIRES 2018, The 2018 Computer Simulation of Radiation Effects in Solids
Shanghai, China, June 18 - 22, 2018

Xu, Z. W.; Song, Y.; Rommel, M.; Liu, T.; Kocher, M.; He, Z. D.; Wang, H.; Yao, B. T.; Liu, L.; Fang, F. Z.:
Raman spectroscopy characterization of ion implanted 4H-SiC and its annealing effects,
ECSCRM 2018, 12th European Conference on Silicon Carbide & Related Materials
Birmingham, UK, September 2 - 6, 2018

Yu, Z.; Zeltner, S.; Boettcher, N.; Rattmann, G.; Leib, J.; Bayer, C. F.; Schletz, A.; Erlbacher, T.; Frey, L.:
Heterogeneous Integration of Vertical GaN Power Transistor on Si Capacitor for DC-DC Converters
ESTC Dresden
Dresden, Germany, September 18, 2018

Zoerner, A.; Oertel, S.; Robert, J.; Dietz, A.:
LPWAN Underground Sensor Network for Optimized Irrigation
IEEE IoT V/T Summit for Agriculture
Siena, Italien, May 9, 2018

NAMES AND DATA

PHD THESES

Bayer, C.:
Untersuchung der elektrischen Feldstärke und des Teilentladungsverhaltens an keramischen Schaltungsträgern

Förthner, M.:
Geprägte Bragg-Gitter Sensoren auf Basis von Hybridpolymeren

Heckel, T.:
Charakterisierung dynamischer Eigenschaften und Modellbildung neuartiger Leistungshalbleiterbauelemente auf Basis von SiC und GaN

Hutzler, A.:
Entwicklung fortschrittlicher Flüssigzellenarchitekturen für leistungsfähige in situ Transmissionselektronenmikroskopie in den Materialwissenschaften

Kraft, S.:
Entwicklung und Charakterisierung eines doppelseitig gekühlten leistungselektronischen Moduls

Rosskopf, A.:
Berechnung von frequenzabhängigen Leistungsverlusten in induktiven Systemen mit Litzenkabeln mittels eines gekoppelten numerischen Ansatzes

Steinberger, M.:
Rückverstromung von wasserstoffhaltigen Gasgemischen in PEM-Brennstoffzellen am Beispiel des Epitaxieabgases

MASTER THESES

Arnet, F.:
Untersuchungen zu zukünftigen Forschungs- und Anwendungsfeldern für die LED-Beleuchtungstechnik (Future Lighting)

Fischer, P.:
Untersuchung der Mikrostruktur von GaN/(Al,Ga)N Multilagenschichten für GaN basierte HEMT-Strukturen

Gruner, S.:
Untersuchung des Facettenwachstums an hochdotierten Silizium-Einkristallen, gezüchtet nach dem Float Zone Verfahren im Doppelellipsoid-Spiegelofen

Hauser, E.:
Charakterisierung und Optimierung eines Kontaktmoduls für elektrische Nervenzellstimulation

Lauterbach, S.:
Charakterisierung des Betriebsverhaltens eines Hybridkältespeichers

Le, P. C.:
Charakterisierung und Modellierung von SiC-Leistungs-MOSFETs

Lei, Y.:
Untersuchung weichmagnetischer Polymere für leistungselektronische Filter

Lipp, M.:
Entwicklung einer Vorrichtung zur Untersuchung des pyroelektrischen Effektes

Merkel, D.:
Untersuchung der morphologischen Eigenschaften von Materialdefekten in 4H-SiC-Epitaxieschichten mittels Rasterkraft-mikroskopie und optischer Profilometrie

Minh Trung, N.:
Entwicklung der Betriebsstrategie für einen Kältespeicher basierend auf Simulationen

Müller, D.:
Untersuchungen zur Wasserstoffqualität innerhalb eines LOHC-basierten Energiespeichers

Pelaic, K.:
Einfluss des dielektrischen Schichtstapels auf die elektrischen Eigenschaften von Silizium-Kondensatoren

Schuck, K.:
Klassifizierung von metallischen Verunreinigungen in Hinblick auf die Beeinträchtigung der elektrischen Materialeigenschaften von PV-Silizium

NAMES AND DATA

BACHELOR THESES

Basu, R.:
Dünnschichttransistoren, Kondensatoren und Widerstände auf flexiblem Substrat

Brunnthaler, J.:
Entwicklung von Methoden zur Optimierung der Barrierewirkung einer SiO2-basierten Diffusionssperrschicht für die gerichtete Erstarrung von PV-Silizium

Dreher, V.:
Einfluss von Druckparametern auf physikalische Eigenschaften von Siebdruckpasten

Flohrer, A.:
Optimierung eines Herstellungsprozesses für ein Mikrofluidiksystem zur Partikelgrößenseparation

Gundermann, S.:
Auswertung und Visualisierung von Dioden-Kennwerten durch statistische Datenanalyse

Horter, L.:
Untersuchung des Einflusses der Ringkernprobengröße auf die Verlustleistungsbestimmung weichmagnetischer Polymere

Kölbel, N.:
Untersuchung zur Temperaturabhängigkeit der Detektor-Eigenschaften von 4H-SiC UV-Photodioden

Lang, T.:
Einfluss der Kontaktmetalle auf den richtungsabhängigen Stromfluss in Dünnschichttransistoren mit einer neuartigen Architektur

Lechner, T.:
Sensorelektronik mit niedrigem Leistungsbedarf für mobile Anwendungen

Lipp, M.:
Aufbau und Testung einer Vorrichtung zur pyroelektrischen Stromerzeugung

Merkel, S.:
Evaluation von kapazitiven Messungen zur Untersuchung von Biofilmen

Ngnogue, A.:
Entwurf und Realisierung eines Prüfadapters mit Federkontaktierung für ein Kennlinienmesssystem unter besonderer Beachtung von Leckströmen und Übergangswiderständen

Nguyen, M. A.:
Bestimmung von Design-Richtlinien für Feldring-Randabschlüsse für 4H-SiC-Bauelemente mittels TCAD-Simulationen

Roas, A.:
Analyse und Optimierung der Randüberhöhung bei Imprintprozessen

Schneider, J. G.:
Optimierung der Betriebsstrategie einer Wärmepumpe mittels Simulation

Schröder, F.:
Modifikation eines vorhandenen PCIV-Messplatzes zur temperaturabhängigen Messung von Widerstandsprofilen an SiC-Proben

Schwarberg, J.:
Optimierung der Atomlagenabscheidung von Aluminiumoxidschichten

Strobel, L.:
Entwicklung von Prognosealgorithmen für Kälteleistungen zur Integration in eine Anlagensteuerung (SPS)

Tkotz, S.:
Erstellung und Realisierung eines Sicherheitskonzepts für eine Redox-Flow-Batterie

Wenniger, P.:
Bestimmung der mikroskopischen Dotierstoffkonzentrationsschwankung mittels Spreading Resistance Profiling

Wich, M.:
Charakterisierung und Modellierung des 1/f-Rauschens von SiC-Mosfets

Wittmann, B.:
Experimentelle Untersuchung an PEM-Brennstoffzellen zum Einfluss des Wasserstoffanteils auf das Impedanzspektrum

Zimmermann, L.:
Kathodenzerstäubung von Indium-Gallium-Zink-Oxid als Halbleiter in Dünnschichttransistoren

Zühlke, R.-H.:
Optimierung der Mehrlagenmetallisierung für SiC-CMOS-Prozesse